PRINCETON APPLIED RESEARCH®

INSTRUCTION MANUAL

WAVEFORM EDUCTOR*

MODEL TDH-9

MP MASTER
MA24618

PRINCETON APPLIED RESEARCH CORPORATION

PRINCETON, NEW JERSEY

INSTRUCTION MANUAL

WAVEFORM EDUCTOR*

MODEL TDH-9

THIS MANUAL APPLIES SPECIFICALLY TO MODEL TDH-9 SERIAL NO. 292

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*Patent Pending

5 pieces 2N5447 (Replacement for 2N3702)
Stored in the Eductor, (behind the transformer).
6/4/75 . H. Fujita

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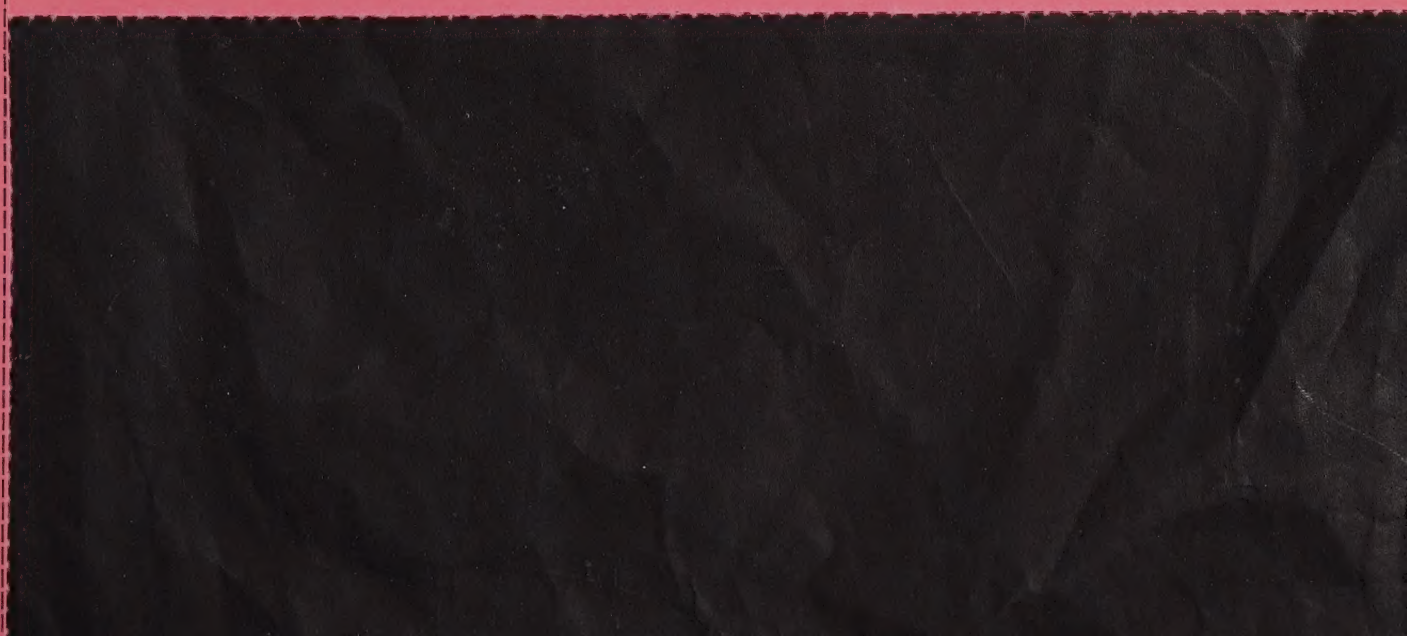

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MANUAL CHANGES

The procedure which appears on page III-6 under "INTERNAL TRIGGER MODE" should read as follows.

(1) Select MIN DELAY and INT Trigger.

(2) Choose a sweep width which brackets the interval of interest.

(3) Trigger the experiment from the trailing (negative going) edge of the TDH-9 gate output.

(4) Operate in the ANALYZE AND READOUT Mode for the required length of time.

(5) Examine the memory contents with an oscilloscope. If a waveform is found, note: (a) the interval between the trigger time and the leading edge of the waveform, and, (2) the duration of the waveform.

(6) Readjust the sweep time so that it equals the duration of the waveform.

(7) Adjust the Delay controls to insert a delay equal to the interval between the trigger time and the leading edge of the waveform.

(8) Make the second run and record the "expanded" waveform.

A number of transistor type changes have taken place as follows.

(1) Signal Board (schematic on page VIII-3)

Transistors Q400, Q403, Q406, Q407, Q408, Q428, and Q430, shown as being type 2N3391A, have been changed to transistor type TIS97.

Transistors Q414 and Q415, shown as being type 2N3566, have been changed to transistor type TIS98.

Transistors Q420, Q422, and Q423, shown as being type 2N3904, have been changed to transistor type TIS97.

(2) Clock Board (schematic on page VIII-5)

Transistors Q300, Q301, Q314, Q317, Q320, Q323, Q325, Q330, and Q331, shown as being type 2N3566, have been changed to type TIS98.

Transistors Q306, Q308, and Q309, shown as being type 2N3904, have been changed to type TIS97.

Transistors Q307 and Q310, shown as being type 2N3391A, have been changed to type TIS97.

(3) Trigger Board (schematic on page VIII-6)

Transistors Q201 and Q204, shown as being type 2N3391A, have been changed to type TIS97.

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Transistors Q205, Q206, Q208, Q209, Q210, Q216, Q218, and Q219, shown as being type 2N3566, have been changed to type TIS98.

Transistors Q202 and Q203, shown as being type 2N3566, have been changed to type TIS97.

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SECTION I
CHARACTERISTICS

1.1 INTRODUCTION

The PAR™* TDH-9 Waveform Eductor™* utilizes an efficient sampling and averaging technique to extract repetitive waveforms from noise. Because the average value of any single point on, or sample of, a signal which consists of a repetitive waveform plus non-synchronous signals and random noise is simply the point value of the repetitive waveform itself (the average value of noise about the point being zero), the TDH-9 can extract, point-by-point, the repetitive waveform from that noise. In essence, the TDH-9 consecutively samples the input signal over 100 equal intervals each time the repetitive waveform occurs, separately integrates the samples to suppress noise, and stores each integrated or "averaged" sample in its memory. With each repetition of the waveform, the contents of the memory asymptotically approach the point-by-point value of the repetitive waveform itself, even though, at the input, this waveform may in fact be completely buried in the noise. Simultaneous with this sampling-averaging process, which is triggered each time the event under study occurs, the Eductor scans its memory and makes the contents thereof available at its output.

Featuring a wide range of time constants, variable gain, precisely adjustable sweep and delay times, and provision for slow readout of stored information to facilitate the use of strip chart or X-Y recorders, the PAR TDH-9 Waveform Eductor is a versatile system which should prove useful wherever the investigation of repetitive events is impeded by the presence of noise.

1.2 THEORY

A signal consisting of a repetitive waveform of interest plus noise is applied to the signal "IN" Jack, and from there through the "COUPLING" Switch and "GAIN" Control to signal channel amplifiers. Following amplification, the signal is fed through a resistor (the value of which depends on the Characteristic Time Constant selected) onto the Signal Bus, which acts as a common line for the 100 memory capacitors. Each memory capacitor is a high-quality, five-microfarad, mylar capacitor, one end of which goes to ground and the other end of which is connected, by way of a series insulated-gate type field-effect transistor, to the Signal Bus. During each sweep, an internal clock oscillator advances a ring counter which controls the memory gates, the gates open consecutively, and each of the memory capacitors in turn is tied to the Signal Bus. If the sweeps are synchronized with the repetitive waveform of interest, that waveform will gradually be "stored" in the memory, because the same portion of the waveform will be applied to any given capacitor on successive sweeps. At the same time, because the signal is being integrated (memory capacitor and characteristic time constant resistor), noise suppression to the degree indicated by the selected time constant will occur. During every sweep, the memory contents are applied to a high input impedance amplifier, further amplified, and finally supplied to the output connectors. Provision is made for "erasing" the mem-

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ory (Signal Bus grounded), and for "delayed" nondestructive (within limits) readout of the memory at speeds completely independent of those used to store the waveform.

Synchronization of the sweep with the external event under study can be effected either externally or internally. For external synchronization, a trigger waveform must be supplied to the Eductor. This trigger waveform causes a Schmitt Trigger to fire, which in turn starts the internal clock. Should delay between triggering and sweep initiation be desired, front panel "DELAY" Controls are provided which allow a delay monostable to be inserted between the Schmitt Trigger and the Clock Oscillator. For internal synchronization, the gate output waveform, derived from a bistable which changes state at the beginning and end of each sweep, must be used to trigger the "event". In internal trigger operation, the clock oscillates continuously and sweeps are successive, unless delay has been selected, in which case the clock stops running for the delay duration after each sweep. Manual triggering, particularly useful when recording, is also provided.

The gate and ramp outputs are derived from a bistable and a Miller Integrator respectively.

1.3 SPECIFICATIONS

SIGNAL CHANNEL

(1) INPUT COUPLING

DC, AC, and GROUND.

(2) INPUT IMPEDANCE

DC - 100 k, AC - 1 microfarad into 100 k ohms.
GROUND - Signal Input Jack disconnected and input circuitry grounded.

(3) VOLTAGE GAIN

Continuously adjustable from 0.4 to 10. Calibrated at one, two, five, and ten.

(4) CHARACTERISTIC TIME CONSTANT

Five to 500 seconds in 1, 2, 5 sequence. The Characteristic Time Constant influences both the degree of noise suppression and the time required for the contents of the TDH-9's memory to "become" the repetitive, synchronous component of the input signal. A shorter time constant gives faster response; a longer time constant, although its use necessitates that the input be averaged over more repetitions, gives better noise rejection.

(5) OVERLOAD CAPABILITIES

With any given setting of the "GAIN" Control, the TDH-9 can withstand, without overloading, signals four times the amplitude required to give full scale, ±10 volts, out.

(6) ZERO ADJUST

±100% of full scale.

(7) RESOLUTION

One percent of sweep time.

(8) SMOOTHING

A switch insertable double section filter with a time constant of 0.5% of sweep time per section is provided to smooth the output waveform pedestals.

TRIGGER CHARACTERISTICS

(1) TRIGGER MODES

External, Internal, and Manual.

(2) TRIGGER REQUIREMENTS

External - Minimum of 500 millivolts peak-to-peak.
Internal - Automatically self triggering.
Manual - Front panel pushbutton switch triggers the sweep.

(3) TRIGGER COUPLING

DC, at an impedance of 10 kilohms.

(4) SLOPE AND THRESHOLD

The TDH-9 is triggerable on either the positive or negative slope of trigger waveforms of either polarity. A "THRESHOLD" Control, adjustable from minus five to plus five volts, permits triggering at any desired point on the trigger waveform.

(5) TRIGGER OUTPUTS

Internal Trigger Mode - A positive five volt gate, suitable for triggering experimental apparatus, is provided during each sweep.
External Trigger Mode - Same as Internal Trigger Mode.
Manual Trigger Mode - Same as Internal Trigger Mode.

DELAY CHARACTERISTICS

(1) DELAY TIMES

Continuously adjustable from ten microseconds to 11 seconds.
Delay accuracy is plus or minus ten percent.

(2) DELAY INSERTION

External Trigger Mode - Delay inserted between triggering and initiation of sweep.
Internal Trigger Mode - Delay inserted between and end of one sweep and the beginning of the next.
Manual Trigger Mode - Same as External Trigger Mode.

(3) DELAY TIME TO SWEEP TIME RATIO (Maximum duty factor)

Can be as great as 11:1.

SWEEP CHARACTERISTICS

(1) SWEEP TIMES

Continuously calibrated and adjustable from 100 microseconds to 11 seconds. A fixed 100 second sweep, to be used only for making recordings, is also provided. Sweep accuracy is ±5%.

OUTPUTS

(1) SIGNAL (Memory) OUTPUTS

Front Panel - ±10 volts at an impedance of 600 ohms.
Rear Panel - Recorder output, suitable for driving most galvanometric or servo type recorders.

(2) GATE

A positive gate pulse at an impedance of 600 ohms is provided for the duration of each sweep. The gate amplitude is five volts ±1%, making it suitable for gain calibration as well as for triggering or gating external equipment.

(3) RAMP OUT

A linear, zero-based, positive going, five volt ramp, with a duration equal to the sweep width, is provided. This ramp, the source impedance of which is 1 k, can be used to drive one axis of an X-Y recorder.

(4) INTERFACE OUTPUTS

All of the output signals, in addition to the TDH-9 power supply voltages, are avilable at a rear panel multi-pin connector to simplify incorporating the TDH-9 into more general systems. Provision is also made at the connector for operating the instrument from external batteries.

OTHER

(1) MEMORY HOLD TIME

The displacement of any pedestal from its level at the beginning of the hold period will not exceed 1% of full scale in 10 minutes at 25°C.

(2) POWER REQUIREMENTS

115 volts AC or 230 volts AC, 50-60 Hz. 25 watts.

(3) ACCESSORIES

PAR Models CR-4 and CR-4A Preamplifiers are available for increasing the input impedance and sensitivity. For further information, please contact the factory or your local PAR representative.

SECTION II
PRELIMINARY INSTRUCTIONS

2.1 GENERAL

COOLING

The TDH-9's solid state construction and low power consumption allow the instrument to be used anywhere the ambient temperature is between 10° and 45° Celsius.

POWER REQUIREMENTS

The TDH-9 operates satisfactorily from either 115 V or 230 V AC at a line frequency of either 50 or 60 Hz; its power consumption is 25 watts.

Transition from 115 to 230 volt operation or vice versa is accomplished by operating a rear panel slide switch. For 115 volt operation, "115" should show in the "window". For 230 volt operation "230" should show.

FUSING

A slo-blo 3 AG 250 volt fuse is installed in the primary circuit of the power transformer. For both 115 volt and 230 volt operation the fuse rating is .5 ampere. In addition to this line fuse, which is located at the rear of the instrument, there are two 3 AG 250 volt fuses rated at .5 ampere located on the plus and minus 24 volt power supply board. Their function is to protect the power supplies.

2.2 FRONT PANEL

INTRODUCTION

The front panel controls, jacks, and indicators are divided into three general groups according to their function. Those on the left either directly affect the instrument's processing of the input signal or determine the mode of operation. The center group allows the operator to select the appropriate trigger and delay functions, and those on the right serve to effect the desired sweep time.

LEFT GROUP

(1) IN JACK

Signals supplied to the signal "IN" Jack are routed through the "COUPLING" Switch and "GAIN" Control to the input amplifier.

(2) COUPLING SWITCH

The "COUPLING" Switch has three positions, "AC", "DC", and "GROUND". In the "AC" position the input signal is coupled through a one microfarad capacitor into 100 k. In the "DC" position the signal

is directly coupled into 100 k ohms. The third position, "GROUND", enables the operator to adjust the "ZERO" Control without having to disconnect the input cable. In this third position, the "IN" Jack is disconnected from the instrument circuitry and the signal channel input is grounded.

(3) ZERO

The "ZERO" Adjust Control, which is located directly to the right of the "COUPLING" Switch, allows DC adjustment of the Eductor's output over a range of plus or minus 100% of full scale out. It may be used in conjunction with DC coupling to suppress the DC component of the input signal, with AC coupling to establish the output waveform baseline at zero, or in conjunction with the "GROUND" position of the "COUPLING" Switch to simply assure that zero in gives zero out. IMPORTANT: This control is effective only when the Eductor is sweeping and operating in the "ANALYZE AND READOUT" Mode. The output of the Eductor in the quiescent state, regardless of the setting of the "ZERO" Control, will be within 0.5% of zero. Similarly, when the Eductor is operating in the "ERASE" Mode and sweeping, the contents of the memory are reduced to zero and not to a level determined by the "ZERO" Control. The "ZERO" Control is also ineffective in the "READOUT ONLY" Mode of operation.

(4) GAIN

The "GAIN" Control is a dual concentric switch-pot combination control which provides continuously adjustable voltage gains from times 0.4 to times ten. When the red inner vernier knob is fully clockwise, the gains selected with the outer black selector, "1", "2", "5", and "10" are calibrated. With the vernier in any position other than fully clockwise, the gain will be uncalibrated and less than the value indicated by the outer knob. The vernier's range of adjustment (0.4 times to 1.0 times the selected gain) is sufficient to assure overlapping ranges.

(5) MODE

Directly to the right of the "GAIN" Control is the "MODE" Switch, which is used to select any one of the instrument's three possible modes of operation, "ANALYZE AND READOUT", "READOUT ONLY", and "ERASE".

In the "ANALYZE AND READOUT" position, the instrument simultaneously samples the input signal, stores the repetitive synchronized components of the signal in its memory, and supplies that stored information to the output. Non-synchronous signal (noise) is suppressed, the degree of suppression being a function of the magnitude of the Characteristic Time Constant and the sweep time.

In the "READOUT ONLY" Mode, no further sampling of the input signal occurs. The instrument simply scans its memory and supplies the contents thereof to the output at the sweep rate. This mode is parti-

cularly useful when used in conjunction with the fixed 100 second sweep time; because it allows such "slow" recording instruments as strip chart and X-Y chart recorders to be used in making permanent records of data recovered at prohibitively high sweep rates. Alternatively, one can readout at faster sweep rates (1 millisecond through 100 milliseconds) using an oscilloscope, and photograph the oscilloscope display to obtain a permanent record. It is important to note that the sweep time that one chooses for readout need only take into account the instruments available for readout (strip chart recorder, X-Y recorder, oscilloscope). The sweep rate used for data analysis has no bearing whatsoever on the choice of sweep rate for readout.

The third or "ERASE" Mode of operation is used when there is no further need for the information stored in the TDH-9's memory. Although the time required to erase is independent of Characteristic Time Constant, it is nevertheless a function of the duty factor, because erasing can occur only when the instrument is sweeping. As a result, the shortest erase times will be achieved when the time between consecutive sweeps is held to a minimum; this is realized by operating with a combination of "INT" Trigger Mode and "MIN" Delay.

(6) CHARACTERISTIC TIME CONSTANT

The last control in the left hand group is the "CHARACTERISTIC TIME CONSTANT" Switch, with which one can select time constants from five to 500 seconds in 1, 2, 5 sequence. The Characteristic Time Constant directly determines the time required for the Eductor to store the repetitive waveform component of the input signal in its memory, with the restriction that this time is actual instrument integrating or sweeping time, and will differ from real or "clock" time by the duty factor.

(7) OVERLOAD LAMP

A red signal "OVERLOAD" indicator lamp, located near the upper edge of the front panel indicates that signal channel overload is occurring (see "GAIN AND OVERLOAD", page III-9).

(8) OUT JACK

Each time the TDH-9 sweeps, the memory contents appear at the "SIGNAL OUT" Jack at an impedance of 600 ohms.

CENTER GROUP

(1) TRIGGER MODE

With the "TRIGGER" Mode Switch, the upper right hand control of the center group, the operator can choose any one of the instrument's three modes of triggering, "EXT", "INT", and "MANUAL".

Of the three modes, the "EXT" Mode is most suitable for general application where the instrument is analyzing and reading out and the

repetition rate of the event under study is externally determined. To use the Eductor in this mode, the experimenter must supply to it a trigger which has a constant time relationship to the repetitive event being studied. Each time this trigger is applied to the Trigger In Jack (lower left in the center group area), one sweep will occur and the Eductor will "examine" that portion of the input signal which is time bracketed by the sweep. If, after the Eductor is triggered, a second trigger should arrive before completion of that sweep initiated by the first, the instrument will "ignore" the second trigger; the TDH-9 is insensitive to any trigger waveforms which arrive when it is active.

Sometimes it may be desirable to use the Eductor itself to trigger the repetitive event under study. This can be done by selecting the "INT" Mode of triggering. In this mode the instrument is self triggering; immediately after one sweep ends, another begins (assuming "MIN" Delay). An advantage of operating the instrument in the "INT" Mode is that the "dead" time will be minimized, and, as a result, the repetitive waveform will be recovered as rapidly as possible for any given combination of Delay and Characteristic Time Constant. Similarly, erasing will be fastest when operating in the Internal Trigger Mode with minimum delay. When operating in this Mode, the positive five volt "GATE" Signal can be used to effect synchronization with external equipment.

The TDH-9 can also be triggered by placing the "TRIGGER" Mode Switch in the "MANUAL" position and then depressing the Manual Trigger Pushbutton Switch. If the instrument is operating in the "READOUT ONLY" Mode, the switch will have to be actuated twice to trigger a sweep. When operating in either the "ANALYZE AND READOUT" or "ERASE" Modes, one "push" will suffice. It is particularly advantageous to use Manual Triggering in conjunction with the "READOUT ONLY" Mode of operation to make a recording. Calibration of an X-Y recorder under these conditions is facilitated because of the "logic linkage" which exists between the Manual Trigger Pushbutton Switch and the "ramp" circuitry. When the instrument is quiescent, the Ramp Output Voltage holds at its maximum level and "full scale" calibration of the recorder can easily be checked. Pushing the switch the first time resets the ramp so that zero can be checked. The second time the switch is actuated, a sweep begins and the ramp output voltage moves linearly toward its maximum value, which it reaches coincident with the end of the sweep. It then holds at that maximum value until such time as the instrument is triggered again.

(2) SLOPE AND THRESHOLD

The dual concentric "SLOPE THRESHOLD" Control, located directly above the Trigger "IN" Jack permits triggering the Eductor with a wide range of possible trigger waveforms. To trigger on either the positive or negative slope of the trigger waveform, one has only to select, with the black outer knob of the control "+" or "-", whichever is appropriate. With the red inner "THRESHOLD" knob, the operator can predetermine at what point on the waveform triggering will occur; the

range of the "THRESHOLD" adjustment is ± five volts. By setting the "THRESHOLD" well above the level of any "noise" which may accompany the trigger waveform, reliable triggering is assured.

(3) IN JACK

This is the only jack in the center group. To trigger the Eductor when operating in the "EXT" Trigger Mode, one must supply an externally derived trigger waveform (minimum amplitude, 0.5 volts peak-to-peak) to the trigger "IN" Jack (10 k input impedance).

(4) DELAY

To the right of the "SLOPE THRESHOLD" Control, and spaced equally above and below it, are the two "DELAY" Controls, which work together to allow selection of 10% accurate delays from ten microseconds to 11 seconds. The effect of the delay controls depends on which trigger mode is being utilized. In the "EXT" and "MANUAL" Modes, the delay is inserted between triggering and the initiation of the sweep. In the "INT" Mode, the delay is inserted between the end of one sweep and the beginning of the next. The delay obtained will be the product of the figures indicated by the two delay controls, except when the lower delay control is in the "MIN DELAY" position, where the delay will be less than two percent of the sweep time.

(5) POWER SWITCH

The "POWER" Switch and its associated indicator lamp are located between the center and right control groups. When the switch is in the "OFF" position, one side of the line is open.

RIGHT GROUP

(1) SWEEP DURATION

The two controls in the right group allow selection of continuously adjustable five percent accurate sweep times from 100 microseconds to 11 seconds. The lower selector is used to determine the range, "X100 μS", "X1 mS", "X10 mS", "X100 mS", "X1 S", and the fixed "100 SEC." range, the use of which should be restricted to the "READOUT ONLY" Mode of operation. The large upper dial determines the factor by which the sweep time selected by the lower control must be multiplied to obtain the actual sweep time. This applies for all positions of the lower selector except the 100 second fixed sweep position. In this position the upper dial becomes ineffective.

(2) READY LIGHT

The "READY" Light, which is located in the upper left-hand corner of the right group area, lights whenever the Eductor is receptive to triggering. As soon as the Eductor is triggered the "READY" Light goes out and remains out for the duration of the sweep. It relights as soon as the sweep is finished. At higher repetition rates, the

light's average brightness will be roughly inversely proportional to the duty factor and indicates an approximation of that quantity.

When the TDH-9 is first turned on, the "READY" Light may not come on, indicating that the bistable which controls this light is in the wrong state. All that is necessary to establish the proper quiescent state is to initiate a sweep, either by momentarily selecting "INT" with the Trigger Mode Switch, or, after selecting "MANUAL" with that switch, by depressing the Manual Trigger Pushbutton. At the end of the sweep, the Ready Light will come on.

(3) GATE AND RAMP OUTPUTS

There are two jacks in the right group area. They are: (1) the "GATE" out jack, and (2) the "RAMP" out jack. For the duration of each sweep an output is available at each of these jacks. The "GATE" out signal, which has a 600 ohm source impedance, is a positive five volt level useful for controlling appropriate aspects of the experiment, and the "RAMP" output (1 k source impedance) is a five volt, positive-going, zero-based, linear ramp, particularly useful for driving one axis (usually horizontal) of an X-Y plotter. Calibration of the horizontal drive sensitivity of an X-Y recorder is particularly easy when it is done while operating with a combination of the "MANUAL" Trigger and "READOUT ONLY" Modes. As mentioned earlier, when using this combination of control settings, the Manual Trigger Pushbutton Switch must be depressed twice to initiate a sweep. The first "push" resets the ramp out signal, and the second triggers the sweep. In the time between sweeps, the output ramp holds at its maximum value until the Manual Trigger Pushbutton Switch is actuated, thereby allowing the operator as much time as is necessary to properly set the horizontal deflection sensitivity of his recorder. Actuating the switch the first time resets the ramp, and, because a sweep will not begin until the button is pushed the second time, horizontal zero can be readily checked. When the second actuation occurs the Eductor scans its memory and the contents thereof will be recorded. At the end of the sweep time the ramp will again hold at its final five volt level. Besides simplifying recorder calibration, this hold characteristic of the ramp output gives the additional advantage of eliminating the problem of automatic ramp resetting causing a retrace line through the finished recording.

2.3 REAR PANEL

SMOOTHING

Because the TDH-9's memory consists of 100 separate channels, the stored waveform will not be continuous, but will instead comprise 100 consecutive discrete levels or pedestals of equal width. The "SMOOTHING" Switch, which is located at the rear of the instrument, provides the operator with the option of either reading out the stored waveform as is, i.e., made up of 100 discrete levels, or, by routing the stored waveform through an internal RC integrating filter, as a smooth continuous waveform. Because the filter is made up of two sections, each of which has a time constant equal to 0.5% of the sweep

time, election of the smoothing option will result in some phase shift and attenuation of high frequencies. Typically, a sine wave of ten cycles per sweep duration will be attenuated 10% and phase shifted about 35 degrees.

RECORDER OUTPUT

Also located at the rear are the two "RECORDER OUTPUT" binding posts. During each sweep, the memory contents are made available at the red binding post. The black binding post is grounded. Next to the binding posts is the "RECORDER SENSITIVITY" Control, with which the operator can adjust the output impedance from 22 kilohms to seven kilohms; this range of adjustment is more than adequate for accomodating galvanometric recorders with sensitivities of either 0.5 milliampere or one milliampere. Servo type recorders, normally high impedance voltage sensing devices, with ten volts for full scale deflection sensitivity, can be directly driven from the "RECORDER OUTPUT" binding posts. The effect of the "RECORDER SENSITIVITY" Control in such cases will be negligible. In those cases where the recorder one wishes to use is more sensitive than ten volts for full scale output, it will be necessary to divide down the output voltage of the Eductor by placing a resistor of appropriate value directly across the input terminals of the recorder. With the "RECORDER SENSITIVITY" Control set at the center of its range, this shunt resistor should be $\frac{14e}{10-e}$ thousands of ohms, where "e" is the input sensitivity of the recorder in terms of volts required at the input to give full scale deflection. With a shunt installed, the "RECORDER SENSITIVITY" Control will allow proportionally greater adjustment of the recorder sensitivity.

PREFILTER SWITCH

Located directly to the right of the Smoothing Switch is the "PREFILTER" Switch, with which the operator can switch the prefilter in or out, according to his needs. For a discussion of the prefilter and its function, see "SIGNAL INPUT CHANNEL", pages IV-1 through IV-3.

INTERFACE OUTPUT

To facilitate the incorporation of the PAR TDH-9 into other more general systems, a connector at which all of the Eductor outputs are available has been provided at the rear panel. Table II-1 indicates which signals are brought out and at which terminal they are available. Provision is also made for operating the Eductor from external batteries by applying plus and minus 31 volts at 350 mA to pins D and E respectively. The 31 volt listed levels are nominal values and can vary as much as 10% without introducing any degradation of the instrument's performance.

PIN	INPUT	OUTPUT
A		GRD
B		+24 } out
C		-24 } out
D	+31 V ±10% at .35 A	} external power in.
E	-31 V ±10% at .35 A	} external power in.
F		SIG OUT
H		~~NO CONNECTION~~ CLK CAP 2/25/74 M.Fujita
J		RAMP OUT
K		GATE OUT
L		NO CONNECTION
M		SWP READY
N		TRIG IN
P		NO CONNECTION
R		CLOCK

Table II-1. REAR CONNECTOR INTERFACE SIGNALS

SECTION III
OPERATING INSTRUCTIONS

3.1 INTRODUCTION

The PAR TDH-9 Waveform Eductor is a sophisticated electronics system useful for the recovery of repetitive waveforms from noise. Because the average value of any single point on, or sample of, a signal consisting of a repetitive waveform plus noise is the point value of the repetitive waveform itself, the TDH-9 can use an efficient sampling and averaging technique to extract, point-by-point, sample-by-sample, the waveform from the noise. The internal organization of the instrument is illustrated in Figure III-1. Note that, independent of the power supply, the instrument comprises four subsystems, the Signal Input Channel, the Memory, the Timing and Memory Control Subsystem, and the Signal Output Channel. The Signal Input Channel primarily amplifies the input signal and prefilters out those components which are beyond the resolution capabilities of the instrument. Front panel controlled functions which are realized through Signal Input Channel circuitry are "GAIN", "ZERO", and "CHARACTERISTIC TIME CONSTANT". What happens to the signal after being processed in the Signal Input Channel depends on the mode of operation. In the "ERASE" Mode the signal will be dead ended, as will be the case in the "READOUT ONLY" Mode. But in the "ANALYZE AND READOUT" Mode, when the Eductor

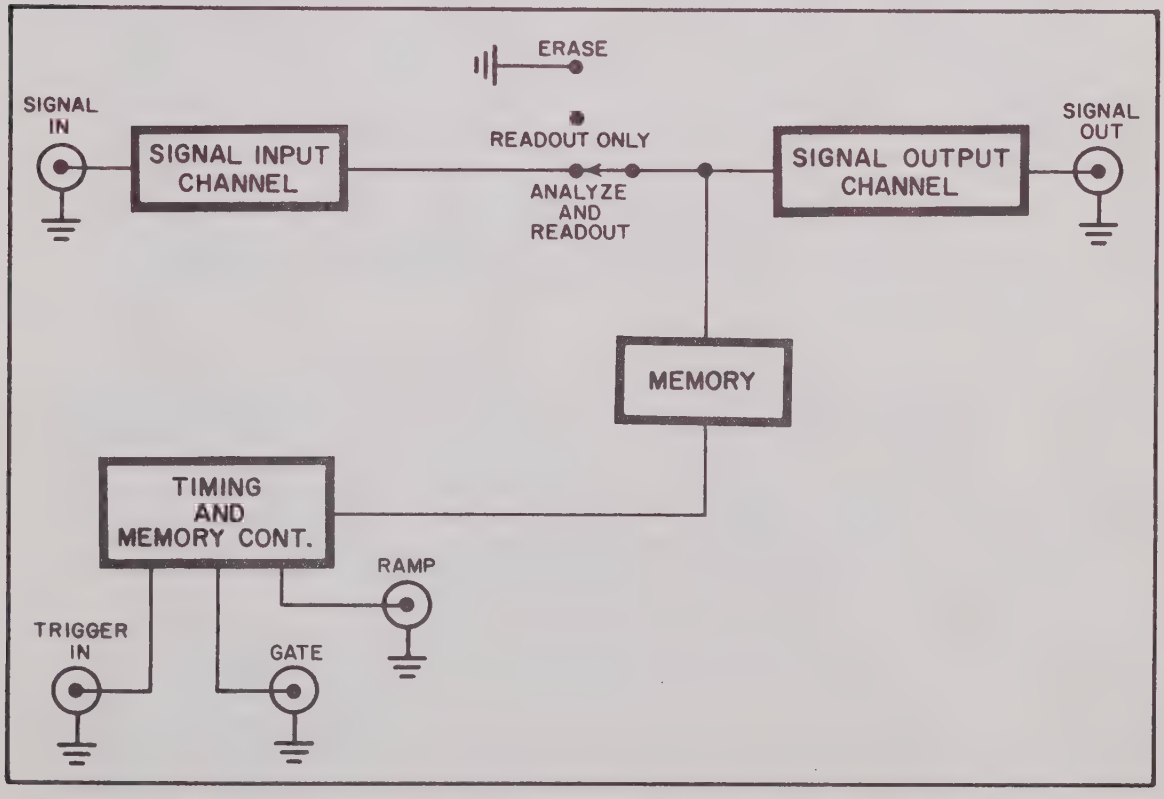

Figure III-1. SIMPLIFIED BLOCK DIAGRAM OF THE TDH-9

is sweeping, the signal will be applied simultaneously to the memory and to the input of the Signal Output Channel. If the Eductor is not sweeping, a crowbar circuit at the input of the Signal Output Channel will short the signal to ground. The memory consists of 100 high quality capacitors, which, each time the instrument sweeps, consecutively "see" the input signal through the resistance determined by the "CHARACTERISTIC TIME CONSTANT" Switch. Because the Eductor is synchronized with the repetitive waveform of interest, the same portion of the input signal will be "seen" by any given memory capacitor on each consecutive sweep, and each capacitor will charge toward the average value of the signal over the particular one percent of sweep time interval that it is gated on. After a sufficient number of sweeps have occurred (the number required being directly proportional to the Characteristic Time Constant), each memory capacitor will have charged to a level corresponding to the amplitude of the repetitive waveform over the appropriate interval, and the synchronized repetitive waveform component of the input signal will have been stored. The signal which is applied to the Signal Output Channel then consists of 100 discrete consecutive pedestals, the amplitudes of which are proportional to the corresponding intervals on the input waveform (even if it is "buried" in noise). The Output Signal Channel provides additional amplification, and, if desired, smoothing of the stored waveform before making it available at the output connectors. Stepping of the memory is effected by the Timing and Memory Control Subsystem, which also determines the Sweep Time (time required to step the memory through the 100 channels), delay duration and insertion, and the Trigger Mode.

3.2 TRIGGERING

INTRODUCTION

The first prerequisite to using the TDH-9 is to synchronize it with the waveform of interest; the time relationship between any point on the waveform and the triggering of the Eductor must be constant. How this synchronization is realized depends on which of the instrument's three trigger modes, "INT", "MANUAL", or "EXT", is being utilized.

MANUAL TRIGGER MODE

Of the three trigger modes, the simplest to use is the Manual Trigger Mode. To trigger the Eductor manually when operating in the "ANALYZE AND READOUT" Mode, one has only to select "MANUAL" triggering with the Trigger Mode Switch and then push the Manual Trigger Pushbutton Switch. Each time the switch is actuated, a sweep will be triggered. Operation in the "READOUT ONLY" Mode differs in that the switch must be depressed twice to trigger a sweep. The first time resets the Ramp Output; the second triggers the sweep.

Because a large number of sweeps must occur to "fill" the memory, any attempt to operate the instrument in the Manual Trigger Mode for the purpose of recovering data will prove to be a tedious process. However, the Manual Trigger Mode is the trigger mode one ought to use when recording, not only because recorder calibration will be greatly facilitated, but also because minimum degradation of a "stored" signal will occur if the instrument is transferred to Manual Trigger operation before going from "ANALYZE AND READOUT" to "READOUT ONLY" operation.

EXTERNAL TRIGGER MODE

Operation of the Eductor in the External Trigger Mode requires that synchronization between the instrument and the input waveform be effected by supplying to the DC coupled Trigger "IN" Jack, a trigger waveform which has a constant time relationship to the repetitive event. Provision is made for considerable latitude as to the size and shape of allowable trigger waveforms. In general, trigger waveforms should be at least 0.5 volts but not more than 50 volts in amplitude, should be at least one microsecond wide, and, if one desires to take full advantage of the "THRESHOLD" adjustment, should be referenced to zero. Additional flexibility is allowed by the combination Slope-Threshold Control. The "SLOPE" Selector permits triggering on either the positive or negative slope of the trigger waveform, and the "THRESHOLD" potentimeter allows one to determine at what amplitude point (within the ±5 volt range of the control) triggering will occur, thereby allowing suppression of DC offset, and discrimination against "noise" which could cause unstable triggering. Because the limit of the Threshold Adjustment is ±5 volts, it becomes ineffective when using trigger waveforms larger than five volts. Similarly, DC offsets greater than five volts cannot be suppressed with the "THRESHOLD" Control and should be avoided.

Indication as to whether or not the Eductor is sweeping is given by the "READY" Light, which is on when the Eductor is quiescent, and out when a sweep is in progress. When the TDH-9 is first turned on, the "READY" Light may not come on, indicating that the bistable which controls this light is in the wrong state. All that is necessary to establish the proper quiescent state is to initiate a sweep, either by momentarily selecting "INT" with the Trigger Mode Switch, or, after selecting "MANUAL" with that switch, by depressing the Manual Trigger Pushbutton. At the end of the sweep, the Ready Light will come on. In general, one might use the following procedure to establish triggering in the External Trigger Mode:

(1) Select "EXT" with the Trigger Mode Switch.

(2) Connect the cable carrying the trigger waveform to the Trigger "IN" Jack.

(3) Select "MIN DELAY" with the Delay Select Switch.

(4) Select the desired trigger slope with the "SLOPE" Selector.

(5) Adjust the "THRESHOLD" Control as required to obtain stable triggering. "Flickering" of the "READY" Light will confirm triggering. At high repetition rates, even though flickering will not be discernable, a decrease in "READY" Light brightness, proportional to the sweep duty factor, will indicate that sweeping is occurring. More precise confirmation is obtainable by using an oscilloscope to observe the "GATE" or "RAMP" Outputs.

INTERNAL TRIGGER MODE

All that is required to trigger the instrument internally is to select "INT" with the Trigger Mode Switch. The Eductor will immediately begin sweeping

at a rate determined by the settings of the Sweep and Delay Controls, as will be evidenced by observing the Sweep "READY" Light. Again, the basic requirement, that the sweeping of the Eductor and the repetitive event be synchronized, must be satisfied. The positive, zero referenced, five volt "GATE" Signal is provided to trigger the external experimental apparatus. The source impedance of this Signal, which begins and ends in step with the sweep, is 600 ohms, and its rise and fall times are less than one microsecond respectively. If delay is selected when triggering internally, it will be inserted between the end of one sweep and the beginning of the next, and the Gate Output will not appear for the duration of the delay time.

3.3 DELAY AND SWEEP

INTRODUCTION

Because the Eductor can "examine" only that portion of the input signal which is time bracketed by the sweep, it is important to select that combination of delay and sweep times which will "dig out" the information of interest. If the operator begins his experiment (assuming External Triggering) without a clear idea of the shape and duration of the waveform he is trying to recover, but believes that a waveform which does not vary from one repetition to the next (independent of noise) is occurring at some fixed time after each trigger, he should first select a sweep width which is sufficiently wide to bracket all of the time between the trigger pulses. By so doing, he will learn from his first "run" where the waveform is occurring with respect to time and what its shape is within the one percent of sweep time resolution capabilities of the Eductor. Once this "general picture" has been obtained, the operator can then easily select that combination of sweep time and delay time which will yield a good, "expanded", more detailed picture of the waveform, provided that he adheres to the duty factor and characteristic time constant restrictions (for a discussion of these restrictions look under "DUTY FACTOR RESTRICTIONS", page III-6). When operating in the Internal Trigger Mode, the problem of selecting proper sweep and delay times is similar, with the exception that, because the repetition rate will be internally determined, different procedures must be followed to calculate the optimum delay time.

In general, the following procedures for selecting proper sweep and delay times should yield good results.

EXTERNAL TRIGGER MODE

(1) Select "MIN DELAY" and "EXT" Trigger.

(2) Establish stable triggering.

(3) Use the two Sweep Time Controls to chose that sweep time which exactly brackets the time between trigger pulses. In so doing, avoid letting the sweep time "overlap" the next trigger pulse. Otherwise, the "overlapped" trigger will be ignored, and, because the instrument consequently will sweep on every other trigger, instead of every trigger, twice as much time will be required to recover the waveform. An easy way to check for trigger "overlap" is to observe the "READY" Light. A sudden increase in brightness or decrease in flicker rate

as the duty factor approaches one, indicates that "overlap" is occurring and that the Sweep Width Vernier should be "backed off" just enough to reestablish proper triggering. Alternatively, one could check for trigger "overlap" by observing the "GATE" Output with an oscilloscope. For a given repetition rate, as the sweep time is increased, the interval between gate pulses will grow shorter and shorter up to the "overlap" point, where a very slight increase in sweep time will cause the interval between successive gates to suddenly "jump" from the minimum value of about two percent of sweep time to a value approximately equal to the sweep time itself.

It may happen that very slow or random trigger repetition rates will make it impossible to select a sweep time which just brackets the interval between triggers. In those cases the operator should choose as his initial sweep time, that one which he believes is most likely to bracket the "waveform of interest".

(4) Operate the instrument in the "ANALYZE AND READOUT" Mode for the appropriate length of time (see "SIGNAL CHANNEL CONTROLS OPERATION", page III-7).

(5) Assuming a waveform is "discovered" which is narrow compared to the sweep time, use the Delay Controls to insert a delay equal to the interval between that slope of the Trigger Waveform which is being used for triggering and the leading edge of the discovered waveform. If the beginning of the sweep and the leading edge of the waveform occur simultaneously, keep the Delay Selector in the "MIN DELAY" position.

(6) Readjust the Sweep Time Controls to obtain a sweep time interval equal to the width of the "discovered" waveform.

(7) If possible, increase the repetition rate of the experiment so that the interval between the trailing edge of the waveform of interest and the "next" trigger pulse is minimized.

(8) Ascertain that the quotient of the Characteristic Time Constant divided by the duty factor does not exceed 5000 seconds. If the duty factor is smaller than that allowed for the particular Characteristic Time Constant being used, it will be necessary to either decrease the Characteristic Time Constant or increase the sweep time until the quotient is brought within limits.

(9) Make the second run.

(10) Transfer to the Manual Trigger Mode.

(11) Transfer to the "READOUT ONLY" Mode.

(12) Record the waveform, using a sweep time appropriate to the recording instrument (oscilloscope, strip chart recorder, X-Y recorder).

INTERNAL TRIGGER MODE See p A1

(1) Select "MIN DELAY" and "INT" Trigger.

(2) Choose a sweep width which brackets the interval of interest.

(3) Operate in the "ANALYZE AND READOUT" Mode for the required length of time.

(4) Examine the memory contents with an oscilloscope. If a waveform is found, note the interval between the trigger time and the leading edge of the waveform.

(5) Readjust the sweep time so that it just brackets the waveform.

(6) If the external experimental apparatus is being triggered by the leading edge of the Eductor Gate Output, use the Delay Controls to insert a delay equal to the difference between the time noted in (4) and the sweep time set in (5). If the external apparatus is being triggered by the trailing edge of the gate pulse, insert a delay equal to the time noted in (4).

(7) Make the second run.

(8) Record the "expanded" waveform.

3.4 DUTY FACTOR RESTRICTIONS

One might conclude from the preceding discussion, that by choosing appropriate delay and sweep times, one could examine not only the waveforms as a whole, but also any given portion of the waveform down to the limits imposed by the one percent resolution and the minimum 100 microsecond sweep time. Although this is largely true, the "hold" characteristics of the memory, although good, are not without limit, and certain duty factor (duty factor being defined as the number obtained when the sweep duration is divided by the sweep period) restrictions must be observed.

The sampling-averaging process which the Eductor uses to recover repetitive waveforms occurs only when the instrument is sweeping. When a sweep is not actually occurring, the memory holds whatever information it may contain. If the time between sweeps is large compared to the sweep duration itself, the demands on the "hold" characteristics of the memory are more stringent than if the time between sweeps is short; there is more time for a significant quantity of charge to leak off the memory capacitors and correspondingly, a greater likelihood of distortion in the stored waveform. The smallest tolerable duty factor at any time is a function of the Characteristic Time Constant. Why the Characteristic Time Constant should have a bearing on the memory hold problem becomes apparent if one considers that the quantity of charge which any given memory capacitor can store during a given sweep is inversely proportional to the Characteristic Time Constant, but that the amount which can leak off, and thereby cause distortion, is more directly proportional to the "off" time. Large values of Characteristic Time Constant give smaller stored charge to leaked charge ratios than do small values,

with the result that the smaller permissible duty factor will be larger with the larger values of Characteristic Time Constant. The relationship between the Characteristic Time Constant and the smallest permissible duty factor is expressed by the following formula:

$$\text{Smallest Permissible Duty Factor} = \frac{\text{Characteristic Time Constant}}{5000}$$

3.5 READOUT ONLY RESTRICTIONS

Distortion of the stored waveform can also occur in the "READOUT ONLY" Mode of operation. When operating in this mode, there are two possible sources of distortion which must be taken into consideration. The first is simple gradual leaking away of the stored waveform, which will not exceed one percent droop in 10 minutes at 25°C. This leakage approximately doubles for each 10°C increase in ambient temperature. The second, which occurs only when the instrument is sweeping, is a simultaneous drooping and phase shifting of the stored signal caused by stray capacity in the memory acting as a "bucket" to dump charge from one memory capacitor to the next as the memory is stepped. The result is, that, after a sufficient number of sweeps have occurred, the stored signal will completely disappear and all of the capacitors will be charged to the same level. Because the "dumping effect" degradation is proportional to the number of sweeps which occur when operating in the "READOUT ONLY" Mode, it will be much more severe with fast sweep times and high repetition rates than with slow sweep times and low repetition rates. With low repetition rates, the dominant effect is leakage, but at high repetition rates the dumping effect degradation predominates and can be quite severe. However, by simply switching from the "EXT" or "INT" Trigger Mode, as the case may be, to the "MANUAL" Trigger Mode, before transferring from "ANALYZE AND READOUT" to "READOUT ONLY" operation, no high repetition rate sweeping in the "READOUT ONLY" Mode can occur, and correspondingly, no dumping effect degradation either. In general then, transition from the "ANALYZE AND READOUT" Mode of operation to the "READOUT ONLY" Mode should be accomplished in the following sequence:

(1) Stop the instrument from sweeping. One convenient means of accomplishing this is to set the Trigger Mode Switch to "MANUAL".

(2) Set the "MODE" Switch to "READOUT ONLY".

(3) Set the Sweep Duration controls to a convenient slow sweep for readout.

(4) Restart the sweep for readout.

3.6 SIGNAL CHANNEL CONTROLS OPERATION

INTRODUCTION

Because the operation of the Signal Channel depends on which mode of operation is being utilized, its operation in each of the three modes will be discussed separately. Also, the operator should be aware that regardless of the mode of operation, none of the Signal Channel Controls will have any visible ef-

fect whatsoever at the output unless the Eductor is sweeping. Whenever a sweep is not actually taking place, the output will be at approximately zero volts.

ANALYZE AND READOUT MODE

COUPLING

The input to the Signal Input Channel is the "SIGNAL IN" Jack. Any signal applied to this jack will be routed to the Signal Input Channel Amplifier by way of the Coupling Switch. The Coupling Switch, in addition to allowing selection of either direct or capacitive input coupling (both at 100 kilohm impedance) with the "DC" and "AC" positions respectively, also offers the operator the choice, by selecting the "GROUND" position, of simultaneously disconnecting the "IN" Jack from the Eductor circuitry and grounding the input of the Signal Input Channel Amplifier.

In the "DC" position, the Eductor will "examine" both the AC and the DC components of the input signal. The DC component of the input signal will appear at the output as a DC offset, the value of which will be equal to the input offset times the gain, as determined by the setting of the "GAIN" Control. If the DC component of the input signal is "large", or of no interest, it will probably be advantageous to select "AC" coupling, though in so doing one should remain aware that the 0.1 second input time constant will roll off the low frequency components at a 6 DB per octave rate beginning at about 1.6 cycles per second. If the input waveform has both low frequency components and an undesirable DC offset, the operator has two choices. The first is to operate with "DC" coupling while using the "ZERO" Control to suppress the input DC, and the second is to use "DC" Coupling with a large external capacitor in series with the "IN" Jack to block the DC. The value of the capacitor in microfarads should be 1.6/f, where "f" is the lowest frequency one wishes to pass. Although using the "ZERO" Control to suppress any input DC is simpler, its use is limited by its range of ±10 volts swing at the output, that is, it cannot suppress any input DC voltage greater than that required to give ten volts out for any given gain. The "GROUND" position of the Coupling Switch is most useful for "setting up" or "zero checking"; the necessity for disconnecting the input cable to remove the signal is eliminated.

ZERO

The "ZERO" Control establishes the reference or baseline DC level at the output. With the exception that its effect can be observed only when sweeping is taking place, it may be compared to the "Vertical Positioning" Control of an oscilloscope. Unlike a "normal" positioning control, however, the response time of the "ZERO" Control is slow. About five times the effective time constant are required for the output to fully respond to any adjustment of the Control (one effective time constant is equal to the Characteristic Time Constant divided by the duty factor). As a result, in adjusting zero, it may be convenient to use a five second time constant and a high duty factor sweep.

GAIN AND OVERLOAD

The TDH-9 not only recovers a repetitive waveform from noise but also amplifies the waveform, as determined by the "GAIN" Control. In general, one should consider two factors in determining the optimum gain for a given experiment. First, the gain must not be so high as to cause "overload", and second, the gain should be as large as possible within the limits set by the overload considerations, in order that the output signal will be as near full scale (±10 volts) amplitude as possible.

In the Signal Input Channel, overload occurs when one exceeds the dynamic range of any of the amplifiers which constitute that subsystem. Because some of these amplifiers are located before the prefilter and some after it, the signal required to overload the Signal Input Channel is a function of both amplitude and frequency. At frequencies below the prefilter roll-off frequency, the amplitude of the signal applied to the input (waveform of interest plus noise, plus DC if DC coupling) must not exceed by more than four times that required to give full scale output. This signal should not exceed 40/G V, plus or minus, where "G" is the "GAIN" Control Setting. Because the red "OVERLOAD" Light will come on whenever low frequency Input Channel overloading is occurring, it is unlikely that overload from this source will cause any serious problems. One might reasonably expect that an "occasional" high noise spike could cause the light to momentarily flicker. Degradation from such occasional input overloading will be negligible. At frequencies above the prefilter roll-off frequency, the overload tolerance is greater. However, this increased noise tolerance is accompanied by a greater likelihood of undetected overload because the prefilter may attenuate high frequencies to such an extent that the overload detect circuitry, which follows the prefilter, will not be activated, even though the amplifiers which precede the prefilter are being overloaded. In those cases where the input signal contains high frequency noise components larger than the limit indicated in Figure III-2, it will be necessary to insert an appropriate low pass filter in front of the Signal "IN" Jack.

The second overload condition arises when the dynamic range of the Signal Output Channel is exceeded, i.e., when the amplitude of the repetitive waveform component of the input signal is sufficiently large to cause output voltage excursions greater than ten volts. To avoid Output Channel overload, one should limit the peak amplitude of the synchronized repetitive component of the input signal to 10/G volts, where "G" is the gain determined by the "GAIN" Control setting. Unfortunately, the noise-to-signal ratio at the input may be so large that it is impossible to know in advance the approximate amplitude of the waveform one is trying to recover. In those cases, the recommended procedure is to monitor the output with an oscilloscope for the duration of the first run. Should the output signal exceed plus or minus ten volts, discontinue the run, select a lower "GAIN" setting, and try again. In actual practice, because the experimenter will probably rapidly learn how large the output signals will be in a given area of investigation, and because the usually encountered noise levels are not so bad as to "totally" mask the waveform, no serious problems should arise from this source of overload induced nonlinearity. The functional relationship between overload tolerance, coherent and noncoherent signal amplitude, and frequency is indicated in Figure III-2.

The second requirement, that the gain be set high enough to give as close to full scale out as possible, comes about because of the instrument's inherent internal noise floor, which typically ranges from less than .1% rms of full scale out at slow sweep speeds to approximately 1% rms of full scale out at the 100 microsecond sweep time (worst case). In maintaining the output signal at or as near full scale as possible, the highest possible output signal-to-noise ratio will be realized for any given sweep speed, and, consequently, the greatest accuracy will be attained.

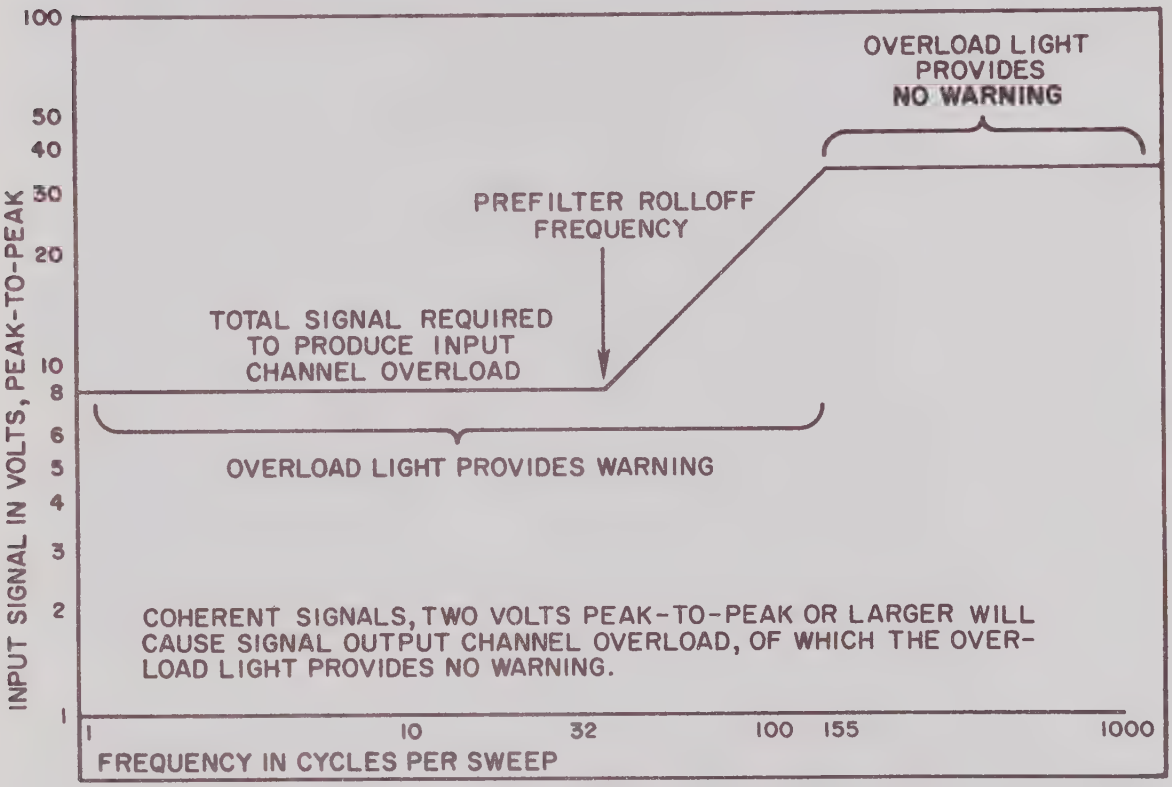

Figure III-2. OVERLOAD TOLERANCE TO COHERENT AND NONCOHERENT SIGNALS AT A GAIN OF TEN (tolerance is proportionally greater at lower gains)

DYNAMIC RANGE

Closely associated with the overload problem is the problem of dynamic range, that is, how large a noise-to-signal ratio at the input can be tolerated? From the preceding discussion of the gain and overload consideration, it is apparent that when the gain is adjusted to give full scale output, the noise-to-signal ratio at the input cannot exceed four-to-one (DC and low frequency noise) without causing Input Channel overloading. Use of the instrument, however, is not restricted to cases where the noise-to-signal ratio at the

input does not exceed four-to-one. Should higher noise-to-signal ratios be encountered, one can reduce the setting of the "GAIN" Control, and by so doing, extend the instrument's dynamic range; at reduced gains larger signals will have to be applied at the input to overload the Signal Input Channel. However, one should bear in mind that the ensuing reduction in output signal amplitude will cause the instrument drift and noise, which are largely independent of gain, to degrade the accuracy of the output signal. The reduction in output signal amplitude can be compensated for simply by increasing the sensitivity of the recording device so as to maintain full scale output, but the increased noise and drift influence cannot be compensated for, and, depending on the amount of noise and drift one is willing to tolerate in the output signal, ultimately determines how far one can go in trading off gain for increased dynamic range. Drift specifications for the TDH-9 are ±20 millivolts per hour and ±10 millivolts per degree Celsius, both referred to output. Assuming that the ambient temperature is stable, drift then will be about 0.2% of full scale out per hour. If the gain is reduced by a factor of ten to increase the dynamic range to 40:1, and increased recorder sensitivity is used to win back full scale output, the 0.2% figure becomes 2%. A 50:1 reduction in gain would yield a 200:1 noise to signal ratio and increase drift effects to 10% per hour, probably an intolerable level in many experiments. The second source of error, internal noise, will often be more of a limiting factor than drift. The predominant internal "noise" in the Eductor arises because the field effect transistor gates vary somewhat in their junction capacity from one to the next. As a result, the memory capacitors, over a large number of sweeps, become slightly charged (independent of signal charge), each to a different level, and it is these "false" memory contents which constitute the Eductor noise. This noise is directly proportional to the Characteristic Time Constant and inversely proportional to the sweep time. Table III-1 indicates the maximum amplitude of this noise as a function of sweep time and Characteristic Time Constant. It clearly shows that one is sharply restricted as to the amount of gain one can trade off for dynamic range with fast sweep times and large characteristic time constants.

Sweep Time	PEAK-TO-PEAK NOISE IN MILLIVOLTS						
	CTC=5 s	CTC=10 s	CTC=20 s	CTC=50 s	CTC=100 s	CTC=200 s	CTC=500 s
100 µs	200 mV	NR	NR	NR	NR	NR	NR
1 ms	20 mV	40 mV	80 mV	200 mV	NR	NR	NR
10 ms	5 mV	5 mV	8 mV	20 mV	40 mV	80 mV	200 mV
100 ms	5 mV	5 mV	5 mV	5 mV	10 mV	20 mV	50 mV
1 s	5 mV	5 mV	5 mV	5 mV	10 mV	20 mV	50 mV
10 s	5 mV	5 mV	5 mV	5 mV	10 mV	20 mV	50 mV

NOTE: These numbers do not include DC drifts.
NR=Not Recommended

Table III-1. TYPICAL INTERNAL NOISE LEVELS AS A FUNCTION OF SWEEP TIME AND CHARACTERISTIC TIME CONSTANT

Although the noise levels may seem high for an information processing instrument, realize that even in the worst case the Eductor can be of great value when put to its intended use, which is to accept an extremely noisy input waveform, suppress the noise, and supply the now only slightly noisy waveform to the output. It is not meant to be a device which improves the signal-to-noise ratio of signals which are only slightly noisy to begin with.

CHARACTERISTIC TIME CONSTANT

Among those factors influenced by the Characteristic Time Constant are the time required to recover a waveform from noise, the amount of signal to noise ratio improvement one can expect, and the amount of internal "noise", which limits dynamic range expansion through gain reduction. Selection of the proper Characteristic Time Constant for a given experiment is particularly important to getting good results. To see why it plays such an important role in determining the instrument's performance, we should briefly consider exactly what is meant by Characteristic Time Constant and how selection of different values of Characteristic Time Constant is effected.

When a signal is applied to the signal "IN" Jack it is coupled into the Signal Input Channel, where it is amplified, prefiltered, amplified again, and then fed through a variable resistor onto the signal bus (by way of the Mode Switch) as illustrated in Figure III-3. When a sweep is occurring, the gates open consecutively and for equal intervals, and the signal at the output of the Signal Input Channel will "see" an integrating network, with a time constant equal to the product of the variable resistor selected with the Time Constant Switch and five microfarads (only one memory capacitor is "in" the circuit at a time).

Selecting different values of Characteristic Time Constant causes different values of resistance to be switched in between the output of the Signal Input Channel and the Signal Bus. Because each gate is on for only one percent of the sweep time, the RC product for any given Characteristic Time Constant will be one percent of the Characteristic Time Constant selected at the front panel.

If the input signal is simple DC, a proportional DC will appear at the output of the Signal Input Channel, and, providing sweeping is occuring, the memory capacitors will begin charging toward the DC at a rate determined by the particular Characteristic Time Constant selected. The instrument active time required to charge the memory to within 1% of the applied voltage will be five times the selected Characteristic Time Constant, but, because instrument active time and real or clock time differ by the duty factor (active time equals the product of the clock time and the duty factor), the real time required to fully charge the memory to the applied DC will be five times the quotient of the Characteristic Time Constant divided by the duty factor, or five times the observed or effective time constant.

Independent of transient considerations, the response of the Eductor to a repetitive waveform with which it is synchronized is very much like its response to a DC voltage. That this should be so becomes apparent when one considers that, relative to the trigger time, any given point on the waveform is a fixed DC voltage. Because any particular memory capacitor always "sees" the same

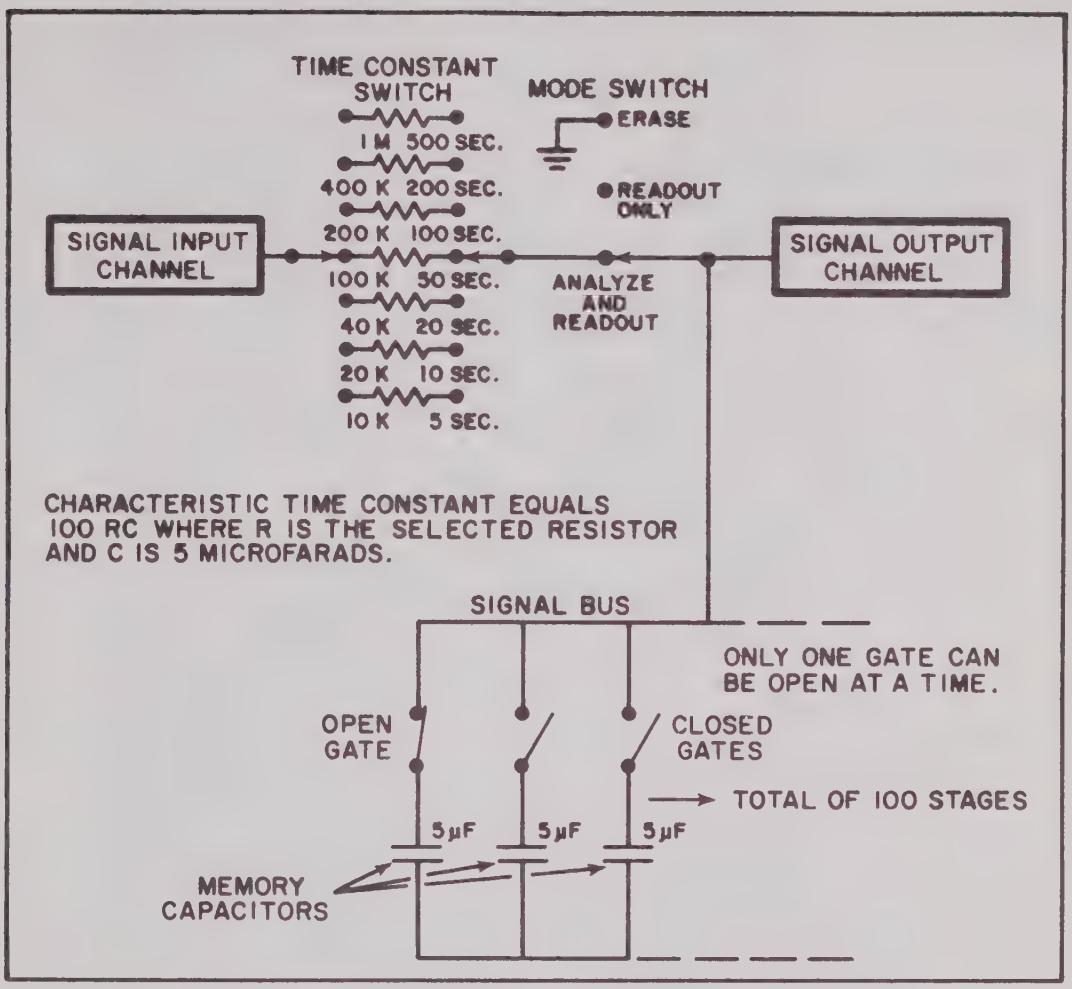

Figure III-3. CHARACTERISTIC TIME CONSTANT CIRCUITRY

point, actually a short one percent of sweep time interval over which the average value approximates the point value, it will charge toward the DC value at that point on the waveform. The memory samples the waveform over 100 consecutive intervals, and each memory capacitor charges toward the particular level which exists for its "on" time. In short, the phase locking of the sweep and the input waveform converts the waveform to a series of DC levels, and each memory capacitor charges to the appropriate DC level. The time required for the memory to completely store the applied waveform is exactly as long as the time required to fully respond to a simple DC input.

Figure III-4 clearly shows the relationship which exists between Characteristic Time Constant, observed time constant, duty factor, and the time required for the Eductor to fully store an input waveform.

The "OPTIMUM ANALYSIS INTERVAL" referred to in Figure III-4 is the time re-

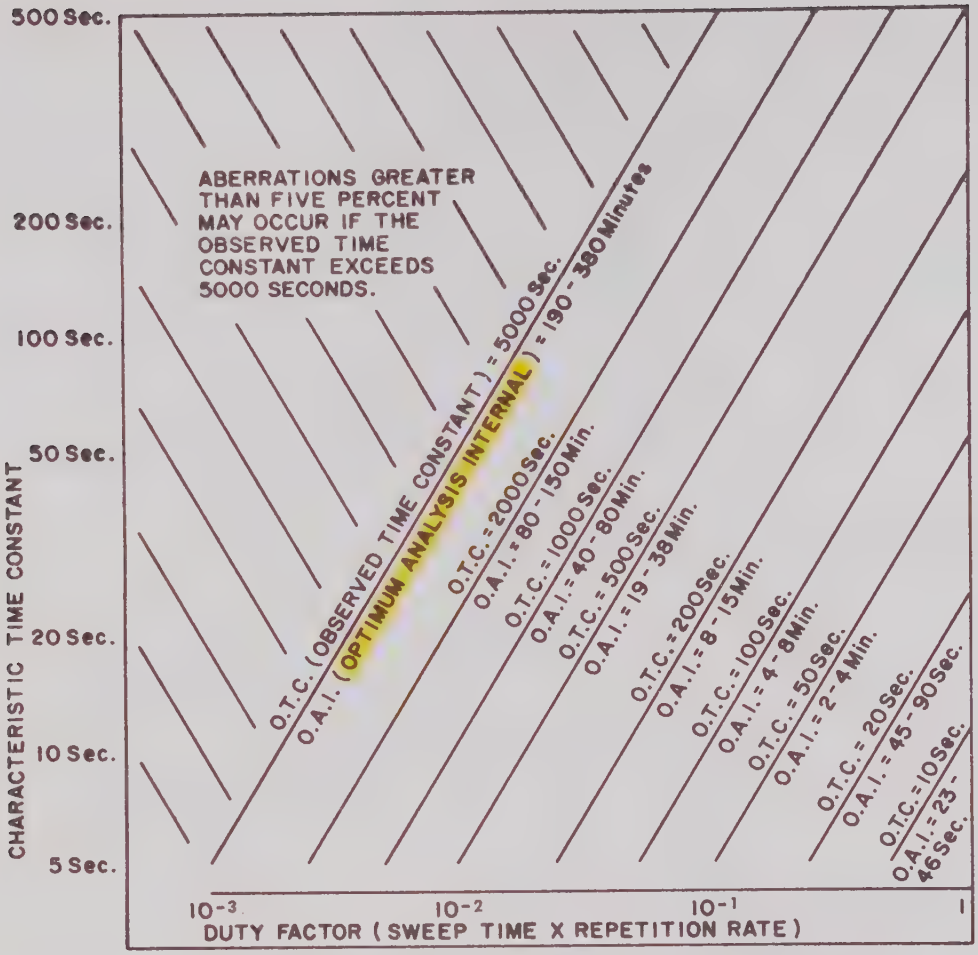
500 Sec.
200 Sec.
100 Sec.
50 Sec.
20 Sec.
10 Sec.
5 Sec.
CHARACTERISTIC TIME CONSTANT
ABERRATIONS GREATER THAN FIVE PERCENT MAY OCCUR IF THE OBSERVED TIME CONSTANT EXCEEDS 5000 SECONDS.
O.T.C. (OBSERVED TIME CONSTANT) = 5000 Sec.
O.A.I. (OPTIMUM ANALYSIS INTERNAL) = 190 - 380 Minutes
O.T.C. = 2000 Sec.
O.A.I. = 80 - 150 Min.
O.T.C. = 1000 Sec.
O.A.I. = 40 - 80 Min.
O.T.C. = 500 Sec.
O.A.I. = 19 - 38 Min.
O.T.C. = 200 Sec.
O.A.I. = 8 - 15 Min.
O.T.C. = 100 Sec.
O.A.I. = 4 - 8 Min.
O.T.C. = 50 Sec.
O.A.I. = 2 - 4 Min.
O.T.C. = 20 Sec.
O.A.I. = 45 - 90 Sec.
O.T.C. = 10 Sec.
O.A.I. = 23 - 46 Sec.
10^-3
10^-2
10^-1
1
DUTY FACTOR (SWEEP TIME X REPETITION RATE)

Figure III-4. ANALYZING TIME AS A FUNCTION OF CHARACTERISTIC TIME CONSTANT AND DUTY FACTOR.

time re-

quired for the memory contents to reach 90% and 99% respectively of their final value. No harm will be done by extending a run beyond the optimum interval, other than the operator will be making inefficient use of his time. Runs shorter than "optimum" will yield not only the most efficient use of time, but also, per unit analyzing time, the biggest improvement is signal-to-noise ratio. However, short runs make signal amplitude determinations difficult. Furthermore, because the full dynamic range of the Signal Output Channel is not being utilized, greater distortion and error will be introduced from internal noise than would be introduced with optimum interval runs. Operation in the "shaded region" (Figure III-4) will reduce the stored charge to leaked charge ratio to the point where leakage degradation to the stored signal becomes significant (see "DUTY FACTOR RESTRICTIONS", page III-6), and consequently should be avoided.

Because the level to which any memory capacitor can charge in one sweep is directly proportional to the sweep duration and inversely proportional to the

Characteristic Time Constant, one can determine the number of sweeps required, as a function of Characteristic Time Constant and sweep time, for the memory to store an input waveform. This point of view becomes particularly advantageous in calculating how much improvement one can expect in signal-to-noise ratio. It can be shown from analysis of commutated-capacitor type comb filters, and the TDH-9 is such a filter, that the signal-to-noise ratio improvement will vary as the square root of the number of sweeps averaged, and furthermore, that the number of sweeps averaged is a function of the Characteristic Time Constant and sweep time. Figure III-5 is a graph which illustrates this functional relationship, and indicates the degree of signal-to-noise ratio improvement one can expect with any particular combination of Characteristic Time Constant and sweep time. It must be emphasized that the number of sweeps averaged figure does NOT refer to the number of sweeps which occur in a given run, but rather indicates, that if a given run comprised an infinite number of sweeps, the memory contents would be the point-by-point average of the input waveform over some preceding number of sweeps, the number being a function of the Characteristic Time Constant, the sweep time, and nothing more. Practically, of course, a run does not last forever, but if its duration is sufficiently long to fall within the "OPTIMUM ANALYSIS INTERVAL" indicated in Figure III-4 the memory contents will be very near the average of the number of sweeps indicated in Figure III-5 and the corresponding improvement in signal-to-noise ratio can be expected.

Note that there are two shaded regions where operation is not recommended. The lower-right shaded region indicates the inadvisability of operating with long sweep times and short Characteristic Time Constants; the memory contents at any time will be the average of the input signal over so few previous sweeps, that little improvement in the signal-to-noise ratio will be achieved. The upper-left shaded area, that of short sweep times and long time constants, indicates those combinations for which the internal noise will exceed 200 millivolts (see "DYNAMIC RANGE", page III-10, and Table III-1, page III-11).

In general then, the choice of Characteristic Time Constant will be restricted by the duty factor and the sweep time. These in turn are functions of the repetition rate of the event under study, the duration of the waveform of interest, the interval between triggering and the time the waveform appears, and the degree the operator wishes to "expand" the waveform. One should choose a value of Characteristic Time Constant which gives an improvement in signal-to-noise ratio sufficient to cause the "signal noise" which appears at the output to be less than the internal noise, being careful to observe that the shaded area restrictions of Figures III-4 and III-5 are adhered to. If, at the faster sweep times, one uses a Characteristic Time Constant much larger than that required to push the signal noise below the internal noise, the unnecessarily increased number of sweeps per run may increase the accumulated internal noise (Table III-1) to where the noise content of the stored waveform is greater than it would have been with a smaller Characteristic Time Constant and a correspondingly shorter run.

Lest this imposing list of restrictions, shaded areas, and warnings cause the operator undue anxiety at the prospect of choosing the proper Characteristic Time Constant, he should realize, that so long as he uses small values of Characteristic Time Constant with short sweep times, large values of Characteristic Time Contant with long sweep times, and keeps the duty factor as

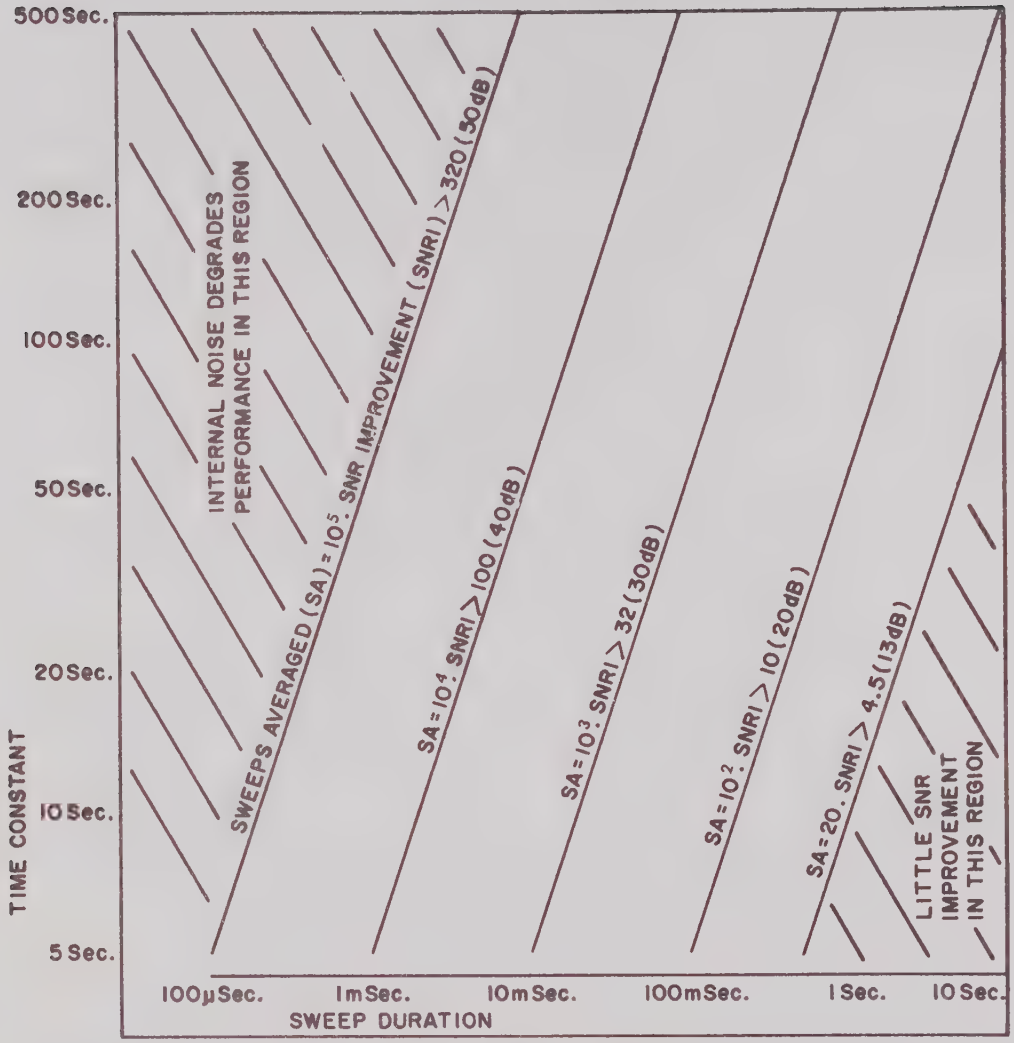

Figure III-5. NUMBER OF SWEEPS AVERAGED AND RMS VOLTAGE SIGNAL-TO-NOISE RATIO IMPROVEMENT AS A FUNCTION OF CHARACTERISTIC TIME CONSTANT AND SWEEP DURATION.

near one as is possible, he can be reasonably sure of getting good results with little difficulty.

SMOOTHING AND FREQUENCY RESPONSE

At the same time that the Signal Input Channel is depositing charge on a given memory capacitor, the Signal Output Channel is sensing the voltage to which the capacitor is charged, amplifying it, and supplying the amplified voltage to the output. The input impedance of the Signal Output Channel is sufficiently high to assure negligible loading of the memory capacitors. At the output, this signal will appear either exactly as it exists in the memory, i.e., as a series of discrete pedestals, or, if the operator introduces the smoothing filter by actuating the rear panel "SMOOTHING" Switch,

as a smooth continuous waveform. Should the smoothing be introduced, one should remain aware that some phase shift and attenuation of higher frequencies will occur. The sine wave response of the filter can readily be calculated (the filter is a two section RC integrator with a time constant per section of 0.5% of sweep time). Typically, a frequency of ten cycles per sweep time will be attenuated 10% and phase shifted 35 degrees at the output. Figures III-6 and III-7 illustrate the transient response of the TDH-9 with and without smoothing. From Figure III-6 it is evident that the transient response (10% to 90% points) without smoothing is about one percent of sweep time. Figure III-7 shows that with smoothing the transient response is lengthened to about 2.7% of the sweep time.

MONITORING

During analyze and readout operation, it is usually worthwhile to monitor the front panel "SIGNAL OUT" Jack with an oscilloscope. By so doing, one can quickly gain some general idea as to the duration and amplitude of the final stored waveform, and perhaps, whether or not the control settings are optimized for the particular experiment being conducted.

READOUT ONLY MODE

INTRODUCTION

In the "READOUT ONLY" Mode, the Signal Input Channel is disconnected from the memory, and all those controls in the front panel left-hand area become ineffective. The Signal Output Channel, however, continues to scan the memory contents with each sweep, and makes those contents available at the output, with or without smoothing as the operator desires. "READOUT ONLY" Mode operation is usually used in conjunction with Manual Triggering to record a stored waveform. In transferring from the "ANALYZE AND READOUT" to the "READOUT ONLY" Mode, be sure to FIRST switch from "INT" or "EXT" triggering, as the case may be, to "MANUAL" triggering. Failure to do so may result in serious degradation of the stored waveform (see "READOUT ONLY RESTRICTIONS", page III-7). Actual recording of the stored waveform should be made as soon as possible after the transfer to manual-triggering and readout-only operation to prevent DC leakage degradation of the stored waveform. No pedestal will droop more than one percent in ten minutes at 25°C and most will droop much less.

RECORDING

The TDH-9 allows considerable flexibility as to the methods which may be used to record a stored waveform. Strip Chart and X-Y recorders, as well as oscilloscope-camera combinations can all be easily used to make permanent records of experimental results. In the "READOUT ONLY" Mode, because the Signal Input Channel is completely disconnected from the memory, the sweep time used to make a recording is in no way determined by the analyze sweep speed; one has only to match the sweep speed to the recording instrument.

(1) STRIP CHART RECORDERS

Of the three recording instruments mentioned above, the strip chart

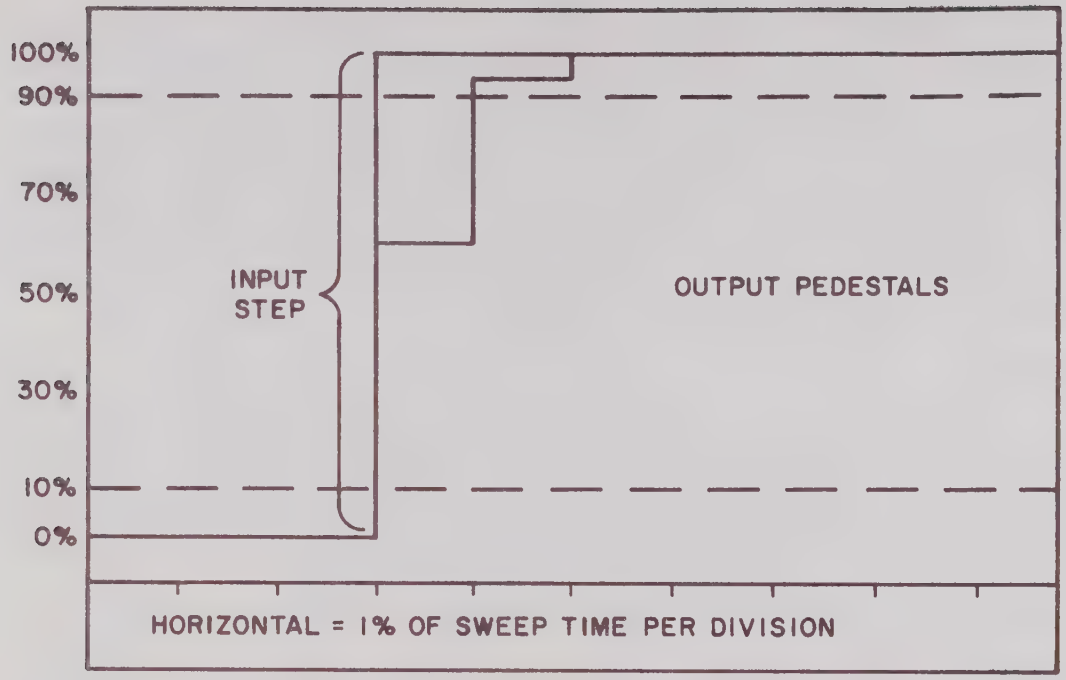

Figure III-6. TRANSIENT RESPONSE WITHOUT SMOOTHING

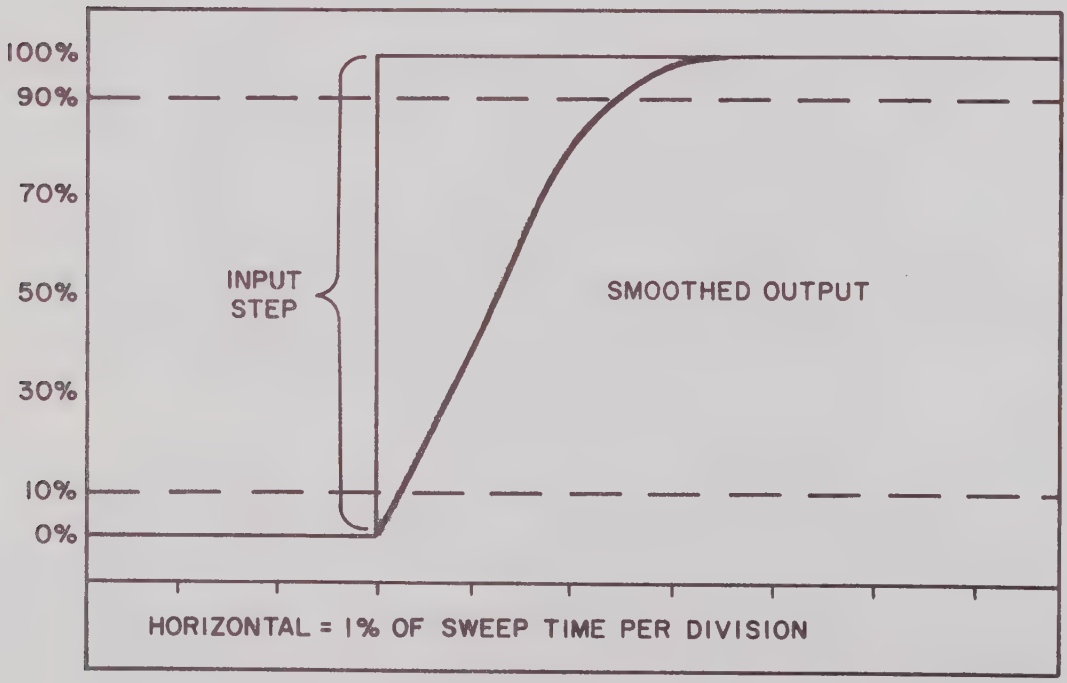

Figure III-7. TRANSIENT RESPONSE WITH SMOOTHING

recorder is the easiest to use. Two factors must be considered in using such a recorder. The first is the recorder's sensitivity and the second is its speed. With reference to sensitivity, strip chart recorders fall into two general types, galvanometric and servo.

Galvanometric recorders are current driven and typically require either 0.5 or 1.0 milliampere of input current for full scale deflection. A single ended "RECORDER OUTPUT", located at the rear of the TDH-9, is suitable for driving such recorders. The full scale output signal is supplied to the red binding post at an impedance which can be adjusted from seven thousand to 22 thousand ohms with the "RECORDER SENSITIVITY" Control. This range of adjustment is adequate for driving any 0.5 mA to 1.0 mA recorder having an impedance of three thousand ohms or less. The black binding post is grounded. To calibrate a strip chart recorder, first supply to the Eductor input a signal which will give full scale Eductor output. Then, adjust the rear "RECORDER SENSITIVITY" Control for full scale deflection of the recorder. The "GATE" signal, five volts ±1%, is especially useful for calibration purposes.

Servo type recorders are usually high-input-impedance, voltage-driven devices. If the servo recorder one intends to use has a ten-volts-for-full-scale-deflection sensitivity range, it can be driven directly from the "RECORDER OUTPUT" Binding Posts. If the recorder is a high sensitivity device, and does not have a ten-volt range, it will be necessary to divide down the Eductor output by placing a resistor across the input terminal of the recorder. With the "RECORDER SENSITIVITY" Control set to the center of its range, this shunt resistor should be $\frac{14e}{10-e}$ thousands of ohms, where "e" is the input sensitivity of the recorder in volts required at the input to give full scale deflection. Final calibration "tweaking" can then be effected with the "RECORDER SENSITIVITY" Control.

As for the second factor, speed, let it suffice to say that the recorder drive speed and the Eductor sweep speed must be compatible. Inasmuch as the slowest Eductor sweep time is 100 seconds, a few of the slower recorders will cause the information loss through "compression" to be so large that they will be practically unusable. With the faster strip chart recorders, one should experience no difficulty in getting good results with the 100 second fixed sweep time.

(2) X-Y RECORDERS

X-Y recorders differ from strip chart recorders in that one must supply them with a "drive" signal. The zero referenced, positive going, five volt "RAMP" Output Signal is intended for that purpose. X-Y recorder calibration is a bit more complicated than strip chart recorder calibration because of the additional drive-signal requirement. However, the Eductor logic is so arranged that when operating with a combination of the "READOUT ONLY" and "MANUAL TRIGGER" Modes, drive calibration becomes very simple. The recommended procedure follows. It should be mentioned, that, to minimize leakage droop degradation, all recorder calibrations should be made before operating

in the "ANALYZE AND READOUT" Mode to store information.

(a) Select "MANUAL" triggering.

(b) Select the "READOUT ONLY" Mode.

(c) Select the sweep speed which will be used to make the recording (usually 100 sec.).

(d) Connect the "RAMP" Output to the recorder horizontal or X axis drive.

(e) Push the Manual Trigger Pushbutton Switch once.

(f) Adjust the recorder horizontal zero as required for zero deflection.

(g) Push the Manual Trigger Pushbutton Switch the second time.

(h) Set the recorder horizontal drive sensitivity for full scale deflection. This adjustment should be made fairly rapidly for good calibration, because the maximum or hold level of the Ramp Signal drifts about 1% per minute with the fixed 100 second sweep time. With faster sweep times the drift is greater. Consequently, whenever possible, use the 100 second sweep time to make X-Y recordings.

The hold feature of the ramp, that it holds at its final value at the end of a sweep instead of resetting to zero, the latter function occurring only after the Manual Trigger Pushbutton Switch is actuated, assures that the operator will have as much time as is necessary to remove the recording or lift the pen; the recording cannot be marred by the "retrace" line.

(3) OSCILLOSCOPES

Alternatively, one can use an oscilloscope in conjunction with a camera to make permanent records. In general, good results will be obtained by driving the oscilloscope signal input from the Eductor front-panel output and by triggering it externally with the Eductor "GATE" Signal. Most oscilloscopes have a sufficiently large range of calibrated vertical sensitivities and horizontal sweep speeds to make their operation with the TDH-9 straightforward.

In selecting an appropriate Eductor sweep time, two factors should be considered. First, the repetition rate and sweep time should be rapid enough to prevent annoying flicker. Second, they should not be so fast as to cause "dumping" effect degradation. By using the "INT" trigger mode and a sweep time of 20 milliseconds, both criteria are satisfied. Nevertheless, it would be wise to keep the Eductor in the "MANUAL" trigger mode when not actually examining or photographing the stored waveform.

ERASE MODE

In the "ERASE" Mode the contents of the memory are rapidly reduced to zero. There are two erasing prerequisites. The Eductor must be in the "ERASE" Mode and it must be sweeping. Approximately five seconds of actual sweeping time is required to erase. Consequently, to erase as rapidly as possible, the duty factor should be large. Fastest erasing will be realized by operating with the "INT" Trigger, "MIN" Delay, and a sweep time of five seconds or faster.

All of the Signal Channel Controls become ineffective in the "ERASE" Mode.

SECTION IV
ORGANIZATION AND CIRCUITRY

4.1 INTRODUCTION

The TDH-9 is divided into five subsystems, called the Signal Input Channel, the Signal Output Channel, the Memory, the Timing and Memory Control Subsystem, and the Power Supply Subsystem. These in turn consist of the various instrument circuits, which are located on the 14 plug-in circuit boards. In this section of the manual, each of the subsystems will be discussed in some detail from a block diagram point of view. Following this discussion, the circuit boards themselves will be treated, with the object of both establishing how they relate to the subsystems and hence to the instrument as a whole, and of explaining their operation on a circuit-by-circuit basis.

4.2 SIGNAL INPUT CHANNEL

Observing Figure IV-1, a block diagram of the Signal Input Channel, note that any signal applied to the Signal "INPUT" Jack is available at the Coupling Switch. What happens to the signal at the Coupling Switch depends on which of the three coupling functions has been selected. In the "AC" position, the signal is capacitively coupled to the switch-attenuator portion of the "GAIN" Control, and in the "DC" position it is directly coupled to that control. The function of the "GROUND" position is twofold. First, the switch-attenuator portion of the "GAIN" Control is grounded to facilitate zero checking. Second, the AC coupling capacitor is precharged to the level of the DC component of the applied signal. As a result, when transferring from DC to AC coupling, precharging will occur, and no transient will be introduced into the signal processing circuits. At the gain selector, that portion of the signal appropriate to the indicated gain is picked off and applied to A1, the input amplifier of the Signal Input Channel.

Besides acting simply as a buffer, this unity-voltage-gain amplifier makes its low impedance output available across the vernier portion of the Gain Control. When the vernier is fully clockwise, all of the signal appearing at the output of A1 will be coupled to A2, and the selected gain will be calibrated. With the vernier in any position other than full clockwise, some lesser portion of the A1 output signal will be coupled to A2, down to a minimum of 40% when the gain vernier is fully counter clockwise.

A2, also a unity-voltage-gain amplifier, provides a constant output impedance to the prefilter, regardless of the setting of the vernier gain control. The prefilter is an RC lowpass filter, the function of which is to remove from the input signal those high frequency components which are beyond the one percent of sweep time resolution capability of the instrument. Because the filter capacitors are mounted on the Sweep Time Selector Switch, such that a different capacitor is selected at each setting of the switch, and the filter resistance is a variable resistor on the same shaft as the Sweep Time Vernier, the prefilter RC time constant product tracks the sweep time, and is always 0.5% of it; a constant relationship is maintained between instrument resolution and the prefilter roll-off frequency. The rear panel Prefilter Switch allows the prefilter to be "removed", if desired.

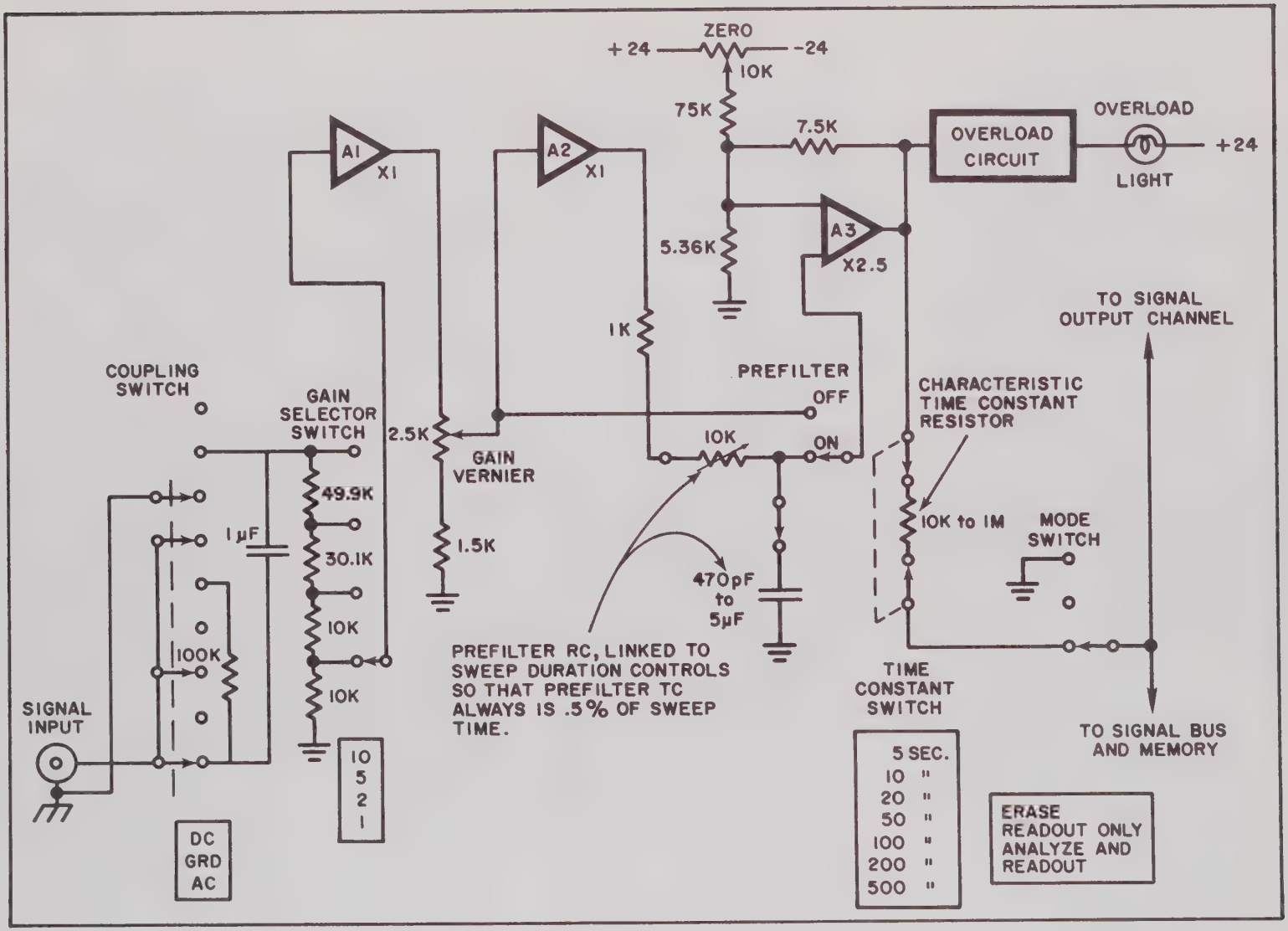

Figure IV-1. BLOCK DIAGRAM OF SIGNAL INPUT CHANNEL

Following prefiltering, the signal is coupled to A3, a non-inverting fedback amplifier with a gain of 2½. Besides amplifying the signal from the prefilter, A3 also adds any DC supplied to it by the front panel "ZERO" Control. The output of A3 will have this DC added to it. A3 drives the Overload Detect Circuit and provides a low impedance output to the Characteristic Time Constant Resistor. The Overload Detect Circuit turns on the Overload Light whenever the output of A3 exceeds plus or minus 12 volts, the dynamic range limit of that amplifier. Because plus or minus 2½ volts are required at the output of A3 to obtain full scale instrument output, it is apparent that for full scale output, the noise-to-signal ratio at the input cannot exceed 4.8:1 (specified at 4:1 to provide a small "cushion") without overloading the Signal Input Channel (see "GAIN AND OVERLOAD", page III-9).

At the end of the Signal Input Channel is the Time Constant Switch, with which different values of resistance are inserted between the output of A3 and (providing the instrument is operating in the "ANALYZE AND READOUT" Mode and sweeping) whichever one of the memory five-microfarad storage capacitors is gated on. The actual RC product of the Characteristic Time Constant Filter is one percent of the value of the Characteristic Time Constant selected at the front panel. This is necessary because each capacitor is in the circuit for only one percent of the sweep time; consequently the contents of the memory approach the synchronized portion of the input signal at the rate one would expect from the selected Characteristic Time Constant and not simply the RC product. Of course, with duty factors less than one, the rate of change of the stored waveform will be that expected with a time constant equal to the Characteristic Time Constant divided by the duty factor. This longer time constant is known as the "observed" or "effective" time constant.

4.3 SIGNAL MODE SWITCH

Coupling between the output of the Signal Input Channel, the Signal Bus, and the Signal Output Channel is effected by the Signal Mode Switch, which allows selection of any one of the three modes of operation, "ANALYZE AND READOUT", "READOUT ONLY", and "ERASE".

In the "ANALYZE AND READOUT" Mode, the Signal Mode Switch channels that signal which appears at the memory end of the characteristic time constant resister to both the Signal Bus and to the input of the Signal Output Channel. If a sweep is occurring, the gates open consecutively for 1% of the sweep time, and each memory capacitor stores the average signal level over the appropriate interval. Simultaneously, this signal will be processed through the Signal Output Channel and will appear at the output connectors. If a sweep is not occurring, no gate will be on, and each memory capacitor will remain charged to whatever level it is at. At the same time a "crowbar" action assures that the output will not "bounce around" during the interval between sweeps, but will instead remain at ground potential. A secondary effect is to make all of the Signal Input Channel Controls completely ineffective whenever the instrument is not sweeping.

In the "READOUT ONLY" Mode, the Signal Mode Switch opens the circuit connecting the Time Constant Switch to the Signal Bus and to the Signal Output Channel. Consequently, removing or changing the input signal will induce no change in the stored signal, whether or not the Eductor is sweeping. Each

time the Eductor sweeps, the memory contents will be applied to the Signal Output Channel and consequently will appear at the output. Within the limits of the earlier discussed leakage deterioration and dumping effect degradation, this readout is nondestructive. Whenever a sweep is not occurring, the crowbar circuit maintains the Eductor output at ground potential.

In the "ERASE" Mode, the Signal Bus is shorted to ground. Having the Signal Bus shorted to ground, however, does not suffice to effect erasing; the instrument must be sweeping. If it is not sweeping, the gates will be closed and the memory capacitors will simply retain their stored charge. About five seconds of sweeping time is required to erase. Erasing will be quickest when using a combination of "INT" Trigger, "MIN" Delay, and a sweep time of one second or faster.

MEMORY

The heart of the TDH-9 is the 100 channel capacitor memory (Figure IV-2). Each "channel" consists of a high quality five microfarad mylar capacitor, one end of which is grounded and the other end of which is connected to the Signal Bus through an MOS type field-effect transistor gate. During a sweep, the Timing and Memory Control Subsystem consecutively opens each of the gates for 1% of the sweep time, and the memory capacitors charge toward the average level of the signal ahead of the Time Constant Resistor over the interval for which each is on. After a sufficient number of sweeps have occurred, each capacitor will be fully charged to the average of that voltage applied

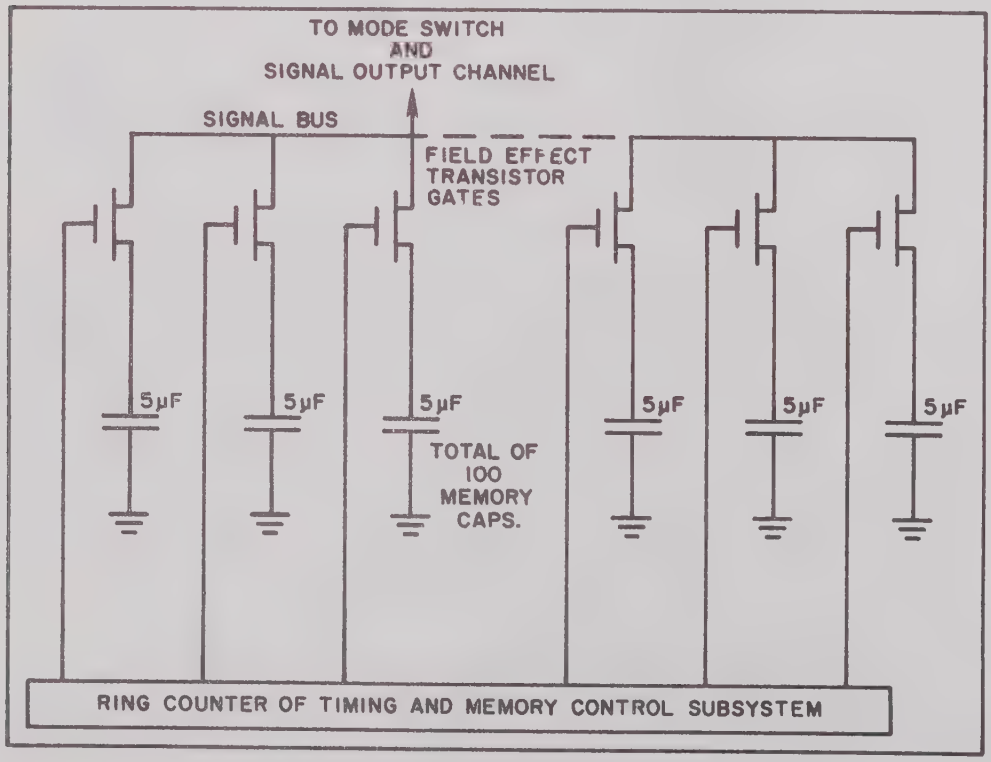

Figure IV-2. MEMORY SUBSYSTEM

to the Time Constant Resistor over the appropriate intervals, and the synchronous portion of the repetitive input signal will have been stored as 100 consecutive voltage levels or pedestals. It is this series of pedestals which is coupled to the input of the Signal Output Channel during each sweep.

4.4 SIGNAL OUTPUT CHANNEL

During any given sweep, the signal on the Signal Bus at any instant will be the voltage to which the "on" memory capacitor is charged at that instant. This signal, which comprises the memory contents, is applied to the input of the Signal Output Channel (Figure IV-3) as the sweep advances. A4, a high input impedance gain of four amplifier, is the first stage of the Signal Output Channel. Besides providing additional gain, this amplifier provides the necessary high impedance buffering between the memory and the remainder of the signal channel circuitry. A field effect transistor crowbar circuit shorts the input of A4 to ground whenever a sweep is not in progress. The extremely high "off" resistance of the field effect transistors assures that the crowbar will not degrade the high input impedance of A4. Two types of compensation are provided at A4. The first is a variable RC from the output of A4 to the input which neutralizes the signal bus capacity. The second is the "FLAT LINE COMPENSATOR", which allows compensation of the capacitor switching effects of the crowbar circuit, thereby assuring that the baseline of the output signal will be flat at the faster sweep times. From the output of A4, the signal is fed to the smoothing switch (located at the rear of the instrument) where it will either be applied to the first section of the smoothing filter, or directly to the output amplifier, A6, depending on whether or not smoothing has been selected. First consider the case where the operator has elected not to smooth. The signal in this case will be applied immediately to the buffer output amplifier A6. Following amplification by A6 (X1), the signal will be available both at the front panel Signal "OUT" Jack at an impedance of 600 ohms, and at the rear panel "RECORDER OUTPUT" binding posts (spaced to accept a standard double banana connector) at an impedance which can be adjusted from 7 k to 22 k with the "RECORDER SENSITIVITY" Control. This unsmoothed signal will consist of 100 discrete pedestals, each of which will be proportional to the average level of the input signal over the 100 corresponding intervals. The absolute amplitude of any pedestal will, of course, also depend on the gain selected at the front panel. Note that all of the gain is provided by amplifiers A3 and A4, and that this gain is always ten. Instrument gains of less than ten are realized by attenuating the input signal, either with the Gain Switch at the input of A1, or with the Gain Vernier at the output of that amplifier.

If the operator has chosen the smoothing option, the signal is not applied directly to A6, but is instead applied to the first section of the smoothing filter, an RC integrator which, in effect, "connects the dots," so that the output signal is no longer "pedestaled" but continuous. The output of the first filter section, following buffering by the unity-voltage-gain amplifier, A5, is fed to the second section of the filter, where more filtering occurs, and then through the Smoothing Switch to the output amplifier, A6. The action from this point is exactly the same as the case without smoothing. Both sections of the smoothing filter are alike and furthermore are identical to the prefilter, that is, the filter components are mounted on the sweep time controls such that the time constant varies as these controls are adjusted, and

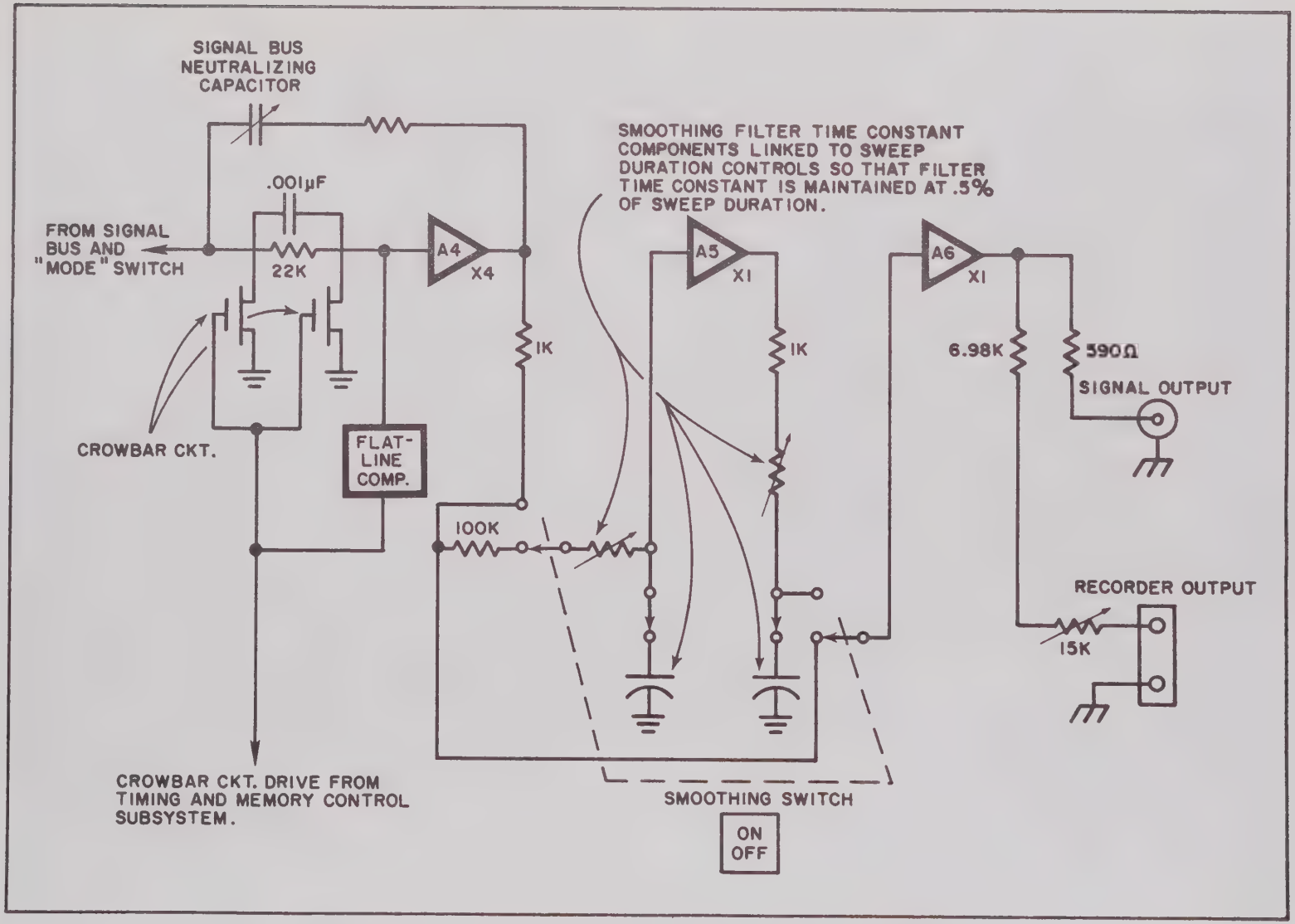

Figure IV-3. BLOCK DIAGRAM OF SIGNAL OUTPUT CHANNEL

the RC product of each section is always 0.5% of the sweep time. The smoothing filter introduces that high-frequency phase shift and attenuation which one would expect from any simple two-section RC low-pass filter. Typically, a frequency of ten cycles per sweep will be attenuated ten percent and phase shifted 35 degrees.

4.5 TIMING AND MEMORY CONTROL SUBSYSTEM

Among the functions of the Timing and Memory Control Subsystem are: (1) stepping the memory, (2) triggering the sweep, (3) determining the sweep and delay durations, and (4) providing the gate and ramp output signals.

The first of these functions, stepping of the memory, is provided by the 102 stage ring counter which sequentially "unlocks" the memory gates. One hundred of the ring stages control the memory gates; the other two perform logic functions. A "clock" oscillator provides the ring counter drive and determines the sweep time. Adjusting the Sweep Time Controls merely varies the frequency of the Clock Oscillator such that the oscillator period is maintained at 1/100 of the selected sweep time. The oscillator is turned on and off by logic circuits which sense the operating condition at any moment, such as the state of the trigger circuits, whether or not delay has been selected, and, whether or not a sweep is occurring. Depending on what those conditions are, the logic circuits will command the Clock to oscillate or not to oscillate, whichever is appropriate.

At this time it would be advantageous to consider the Timing and Memory Control Subsystem in somewhat more detail, for which purpose Figure IV-4, a block diagram of this subsystem, has been provided. Observing Figure IV-4, note that the ring counter stages fall into two groups. The first group controls the memory gates and comprises ring counter stages 001 through 100. The second group, which comprises the two stages 00A and 00B, performs logic functions. Both groups constitute the complete ring counter, which has the following characteristics:

(1) Only one ring stage can be on at a time.

(2) One ring stage must be on at any time.

(3) If one of the memory group stages is on, the memory gate it controls will open and the corresponding memory capacitor will be able to "correct" the voltage to which it is charged.

(4) If one of the logic ring stages is on, the crowbar circuit will ground the input of the Signal Output Channel.

(5) The ring counter states always turn on in sequence, the sequence being 00A, 00B, 001, 002, ---, 100, 00A. 00A is the ring stage which is on when the Eductor is quiescent.

(6) All of the ring stages, logic and memory control, are driven from a common line called the Emitter Bus. Each time a drive pulse is applied to the Emitter Bus, the ring counter will advance one step.

CONTROL LOGIC

There are three logic gates which control the ring counter. They are the "TRIGGER" Gate, the "RUN" Gate, and the "DON'T RUN" Gate. The Trigger Gate, so long as a sweep is not occurring, drives the Emitter Bus directly; the "DON'T RUN" and "RUN" Gates, by turning the Clock Oscillator on and off, control the ring counter.

A sweep is initiated by applying a trigger pulse to input number two of the Trigger Gate (assuming "MANUAL" or "EXT" triggering), which then couples the pulse to the Emitter Bus, advancing the ring counter one step. Input number two of the "DON'T RUN" Gate immediately senses that 00A has gone off and tells the "RUN" Gate, via input number one of that gate, to allow the Clock Oscillator to commence oscillating.

The number one input of the "DON'T RUN" Gate is effective only when the special combination of Manual Trigger and Readout Only is present, in which case the "DON'T RUN" Gate output will not change state until 00B goes off; a second trigger pulse is required to advance the ring from 00B to 001, and thereby start the Clock. Because manual triggering is one of the two requirements for this case, the operator will have to depress the Manual Trigger Pushbutton Switch twice to start the clock and begin a sweep. Realize that if manual triggering is being utilized in conjunction with the "ERASE" or "ANALYZE AND READOUT" Modes, the number one input of the "DON'T RUN" Gate will not be activated, and one need only to depress the Manual Trigger Pushbutton Switch once to start the clock and begin a sweep.

Note that the output of the "RUN" Gate is also coupled to input number one, the inhibit input, of the "TRIGGER" Gate. So long as this inhibit input is activaced, and once activated it will remain so until the sweep it completed and 00A comes on again, the "TRIGGER" Gate will ignore any trigger pulse which may be applied to it. Input number two of the "RUN" Gate is an override input; so long as it is active, its input up, the "RUN" Gate will force the clock to oscillate, regardless of the command coming from the "DON'T RUN" Gate.

There are two modes of override control. In the first mode, which prevails when operating with "INT" trigger and "MIN" delay, switch contacts make which supply positive DC to the override input locking the oscillator on. The TDH-9 sweeps consecutively with the least possible delay between sweeps. Should the Delay Selector be in any position other than "MIN" ("INT" trigger retained), the second override mode prevails and the Delay Monostable output (the Monostable being triggered when ring stage 100 goes off) will drive the override input. For the delay duration, this output, which is quiescently up, will be down and control of the "RUN" Gate will go over to the number one input, stopping the clock. In this way, with internal triggering, the delay is inserted between the end of one sweep and the beginning of the next. When the trigger mode is "EXT" or "MANUAL", the override input is open and the number one input alone controls the clock.

RAMP AND GATE OUTPUTS

The Timing and Memory Control Subsystem produces two output signals, the

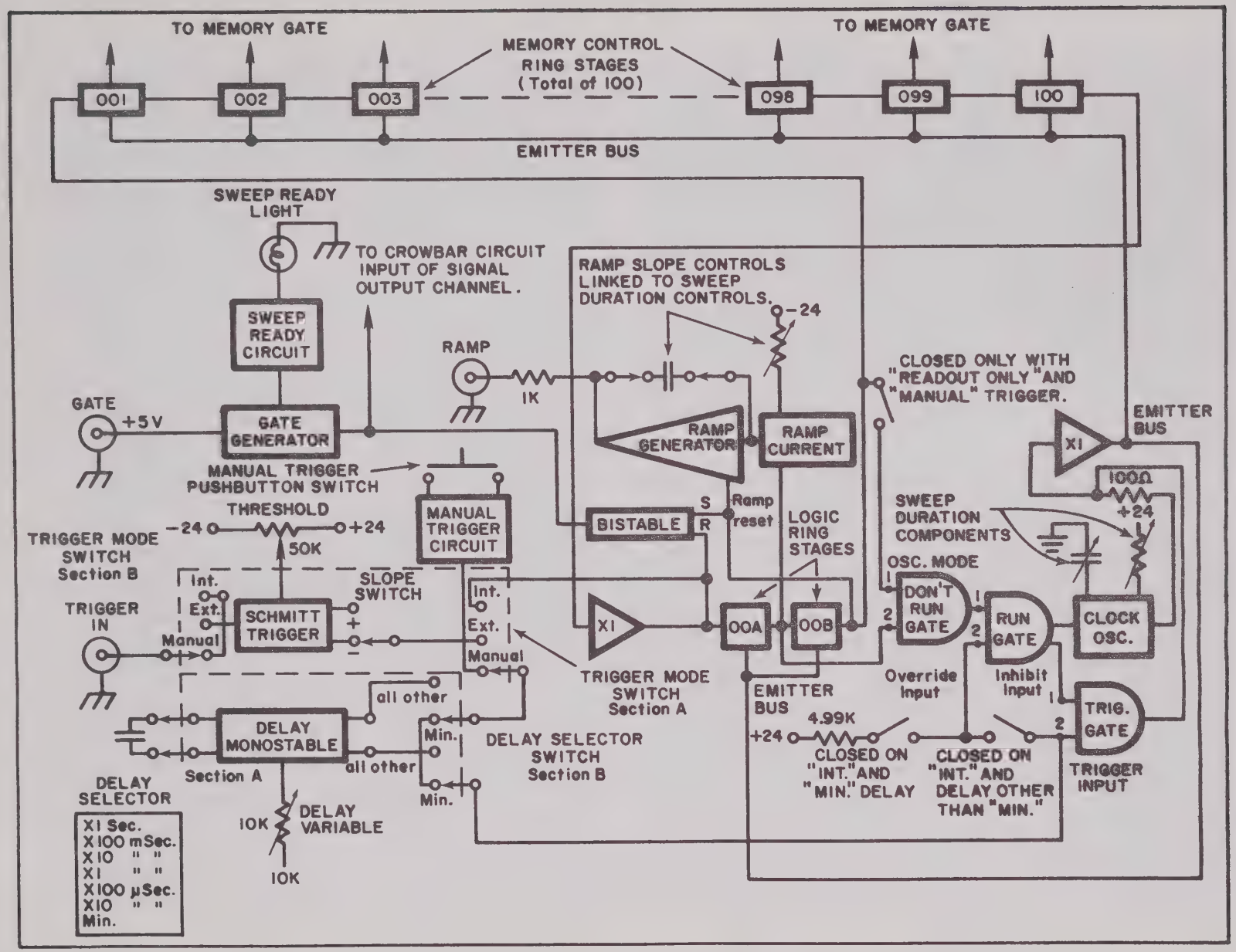

Figure IV-4. BLOCK DIAGRAM OF TIMING AND MEMORY CONTROL SUBSYSTEM

"RAMP" output, which is brought out at the "RAMP" Jack, and the "GATE" output, which is brought out at the "GATE" Jack.

Logic ring stage 00B drives the set input of the bistable which controls the Gate Generator. Whenever 00B goes off, which means a sweep is under way, the bistable is triggered and a gate signal is produced, which, regardless of the Trigger Mode, appears at the "GATE" output Jack for the duration of the sweep. Because ring stage 100, the last memory ring stage, resets the bistable by going off, the gate duration will always be equal to the sweep time.

Ramp production and reset characteristics are a function of the trigger and operating modes. This comes about because the combination of "READOUT ONLY" and "MANUAL" Trigger activates the number one input of the "DON'T RUN" Gate. With all other combinations, only input number two of the "DON'T RUN" Gate is active and different logic conditions prevail.

Regardless of which combination is present, ramp production is always the same to the extent that whenever 00A is on, no ramping current will be available to the Ramp Generator and the ramp output voltage will "hold" within the leakage-drift capabilities of the Ramp Generator (one percent per minute with the fixed 100 second sweep time). If 00A is off, ramping current will be available and a ramp may be produced, depending on whether 00B is on or off. When 00B is on the ramp will be reset, that is, the ramp output voltage will be zero volts (±100 millivolts). Because no ramping current will be available when 00A is on, and because the Ramp Generator is reset when 00B is on, it follows that 00A and 00B both must be off in order for a ramp to be produced, that is, a sweep must be occurring.

Consider the case for any combination other than that of Manual Trigger and Readout Only. In the quiescent state, regardless of the trigger mode, 00A will be on, ramping current will be withheld, and the ramp output will be holding. Furthermore, if one assumes that a previous sweep has occurred, the ramp output will be holding at its maximum, final, or "full scale" value of five volts. Now assume a trigger is supplied to input number two of the Trigger Gate. The action will be the same regardless of the Trigger Mode. After being coupled through the Trigger Gate, the trigger pulse will advance the ring counter one step, from 00A to 00B, and, because the only effective input of the "DON'T RUN" Gate is input number two, the clock will immediately commence oscillating. When 00B comes on, the ramp resets, such reset being completed by the end of the 00B on-time. However, because the clock immediately commences to oscillate, the reset is momentary (00B is on for only one clock period) and the ramp output begins rising linearly toward its final value. It will continue rising until 00A comes on again, at which time the ramping current will be withheld, the ramp will hold, and the reactivation of input number two of the "DON'T RUN" Gate shuts off the Clock Oscillator.

With the Readout Only and Manual Trigger combination, input number one of the "DON'T RUN" Gate becomes effective, with the result that simply advancing the ring from 00A to 00B with a trigger pulse will not suffice to start the clock. Both 00A and 00B will have to be off before the "DON'T RUN" Gate output will change state and the clock will start. To advance the ring from 00A to 00B, the operator will have to depress the Manual Trigger Pushbutton Switch once.

To advance it from 00B to 001 and thereby start the clock, he will have to depress the button a second time. Because with this Manual Trigger, Readout Only combination, 00B remains on, and consequently the ramp output remains reset to zero for as long as the operator desires, he will have as much time as he deems necessary to set the recorder zero control. Correspondingly, because the ramp holds at its maximum value in the quiescent state, adjustment of the horizontal drive sensitivity is equally simple.

The Ramp Generator itself is a Miller Integrator, with the ramp duration determining components ganged with the Sweep Controls, such that the ramp always reaches positive five volts coincident with the end of the sweep.

TRIGGERING

How the Eductor is triggered depends on which trigger mode is being used. In the Manual Trigger Mode, depressing the Manual Trigger Pushbutton Switch causes the Manual Trigger Circuit to generate one trigger pulse. This trigger pulse will either be coupled to the input of the Delay Monostable, or directly to input number two of the Trigger Gate, depending on whether or not the Delay Selector is set to some position other than "MIN". If delay has been selected, the trigger pulse will start the Delay Monostable, and the trailing edge of the monostable output will supply the necessary trigger command to input number two of the Trigger Gate to advance the ring from 00A to 00B. In the "EXT" Trigger Mode, an externally drived trigger waveform must be supplied to the Trigger "IN" Jack to effect triggering. From this jack, the trigger waveform is routed by way of Section B of the Trigger Mode Switch to the Schmitt Trigger, which allows the slope and threshold functions.

The Schmitt output is then coupled to Section A of the Trigger Mode Switch, from where the action is exactly the same as it was in the Manual Trigger case. In the Internal Trigger Mode, the output of the last memory ring stage, stage 100, simultaneously turns logic ring stage 00A on and supplies the trigger command to advance the ring from 00A to 00B and begin a sweep. This trigger command, as was the case for both manual and external triggering, is supplied to Section A of the Trigger Mode Switch. Consequently, if the Delay Selector is not in the "MIN" Delay position, a delay, as determined by the setting of the Delay Controls, will be inserted between the trigger command (stage 100 goes off) and the time an input will appear at the input number two of the Trigger Gate to advance the ring from 00A to 00B and begin a sweep.

DELAY

Regardless of which trigger mode is being employed, the trigger pulse is applied to Section B of the Delay Selector Switch. If that switch is in the "MIN" Delay position, the Delay Monostable will be bypassed, and the trigger pulse will be fed directly to the trigger input of the Trigger Gate. If the Delay Selector is in any other position, the trigger pulse will be fed to the monostable input and not to the Trigger Gate. Because the Delay Monostable output is supplied to the Trigger Gate, triggering will nevertheless occur, but only after the indicated delay time elapses. Note that, in the "INT" Trigger Mode, the monostable output is also used to activate the override input of the "RUN" Gate.

SWEEP CONTROLS

Worthy of special mention are the Sweep Time Controls because of the large number of instrument parameters which are affected by their setting. The upper Sweep Control comprises five separate concentric wirewound potentiometers (wired to act as simple variable resistors), each of which affects a different circuit. Adjusting the control varies not only the sweep duration, but also the prefilter time constant, the time constant of each of the two sections of the smoothing filter, and the ramping current, with the result that the time constant of the three filters is always maintained at 0.5% of the sweep time, and the ramp will always reach the same final voltage. Similarly, the lower Sweep Selector Switch comprises five sections, each of which switches the timing capacitors for the filters, ramps, and sweep circuits respectively, such that, regardless of the switch setting, a constant relationship between time and the affected parameters is maintained.

4.6 POWER SUPPLY

Observing the TDH-9 power supply block diagram, Figure IV-5, note that the instrument can operate from either 115 V or 230 V AC (50 - 60 Hz), and that the changeover is effected by actuating the Line Voltage Selector Switch to put the two transformer primary windings either in parallel (115 volt operation) or in series (230 volt operation).

Following step-down by the transformer, the AC is applied across the bridge, where it is rectified to obtain ±31 volts unregulated DC. This "raw" DC then goes to the Power Supply Board, which furnishes the highly regulated ±24 volts required by the circuit boards. Additional emitter follower type "regulators" develop the "special" ring counter voltages, +3, -7, -9, and -11 volts.

4.7 INTRODUCTION TO CIRCUIT DESCRIPTIONS

The bulk of the circuitry which constitutes the TDH-9 is located on the fourteen plug-in boards, of which there are five kinds. Included are one "TRIGGER" Board, one "SIGNAL AMPLIFIER" Board, one "CLOCK" Board, one "POWER SUPPLY" Board, and ten "GATING AND STORAGE" Boards. Each of these plug-in boards is associated with one or more of the already discussed subsystems.

Components of both the Signal Input and Signal Output Channel Subsystems are located on the Signal Amplifier Board. Elements of the Timing and Memory Control Subsystem are located on the Trigger and Clock Boards. The Gating and Storage Boards comprise circuitry of both the Memory and of the Timing and Memory Control Subsystems. Figure IV-6 illustrates the location of the different plug-in boards.

4.8 SIGNAL AMPLIFIER BOARD

Except for those components which are located at switches and controls, the Signal Amplifier Board may be considered to constitute the Signal Input and Signal Output Channels.

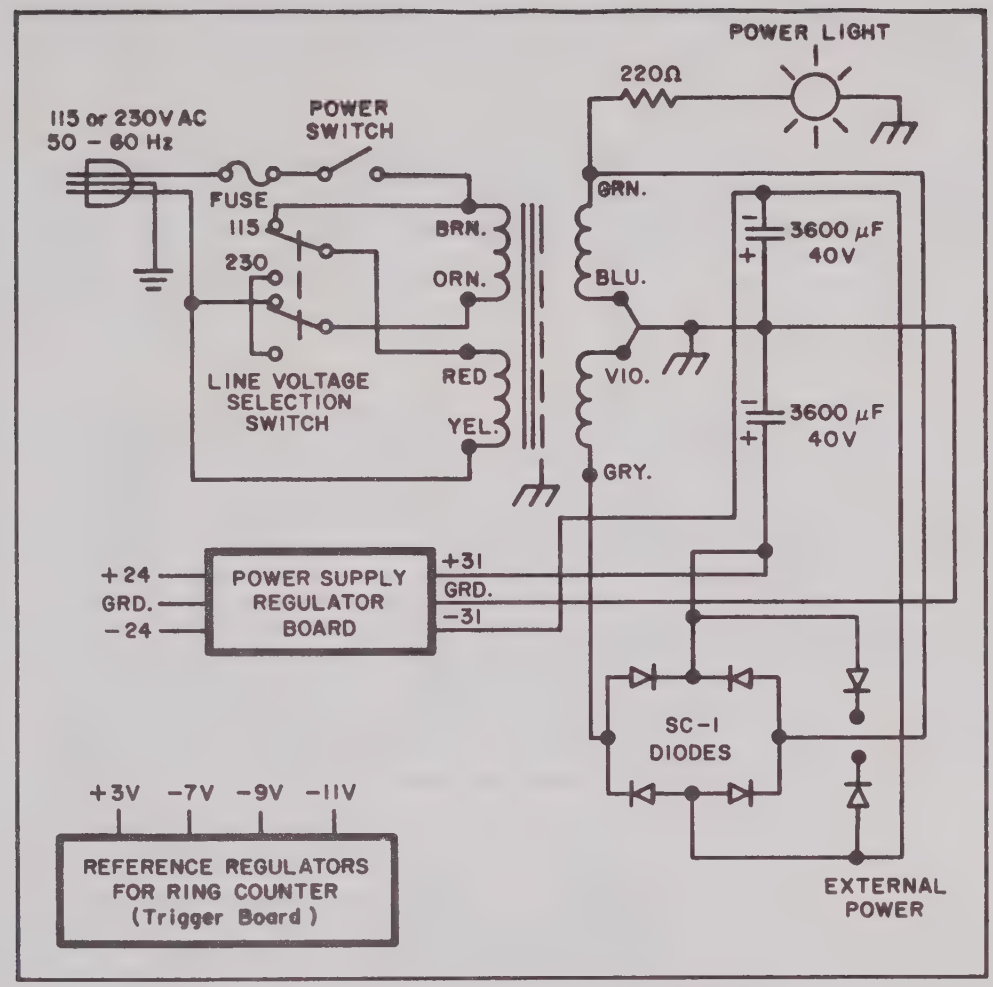

Figure IV-5. POWER SUPPLY SUBSYSTEM

AMPLIFIER A1

Observing the upper left hand corner of the Signal Amplifier Board schematic diagram (page VIII-3), note that A1, the first Signal Input Channel amplifier, is a complementary emitter follower which accepts signals from the step-selector portion of the Gain Control and supplies those signals at a lower impedance to the vernier portion of that control. Considering the amplifier's three transistors, Q400 is the input stage, Q402 the output, and Q401 acts as a constant current source for Q402. There are two timpot adjustments, R400 and R403. R400, by establishing the potential across R402 and thereby the current supplied by this resistor to the base of Q400, assures that no base current will be supplied by the Gain Control. As a result, selecting different gain ranges will incur no DC shift at the input of A1.

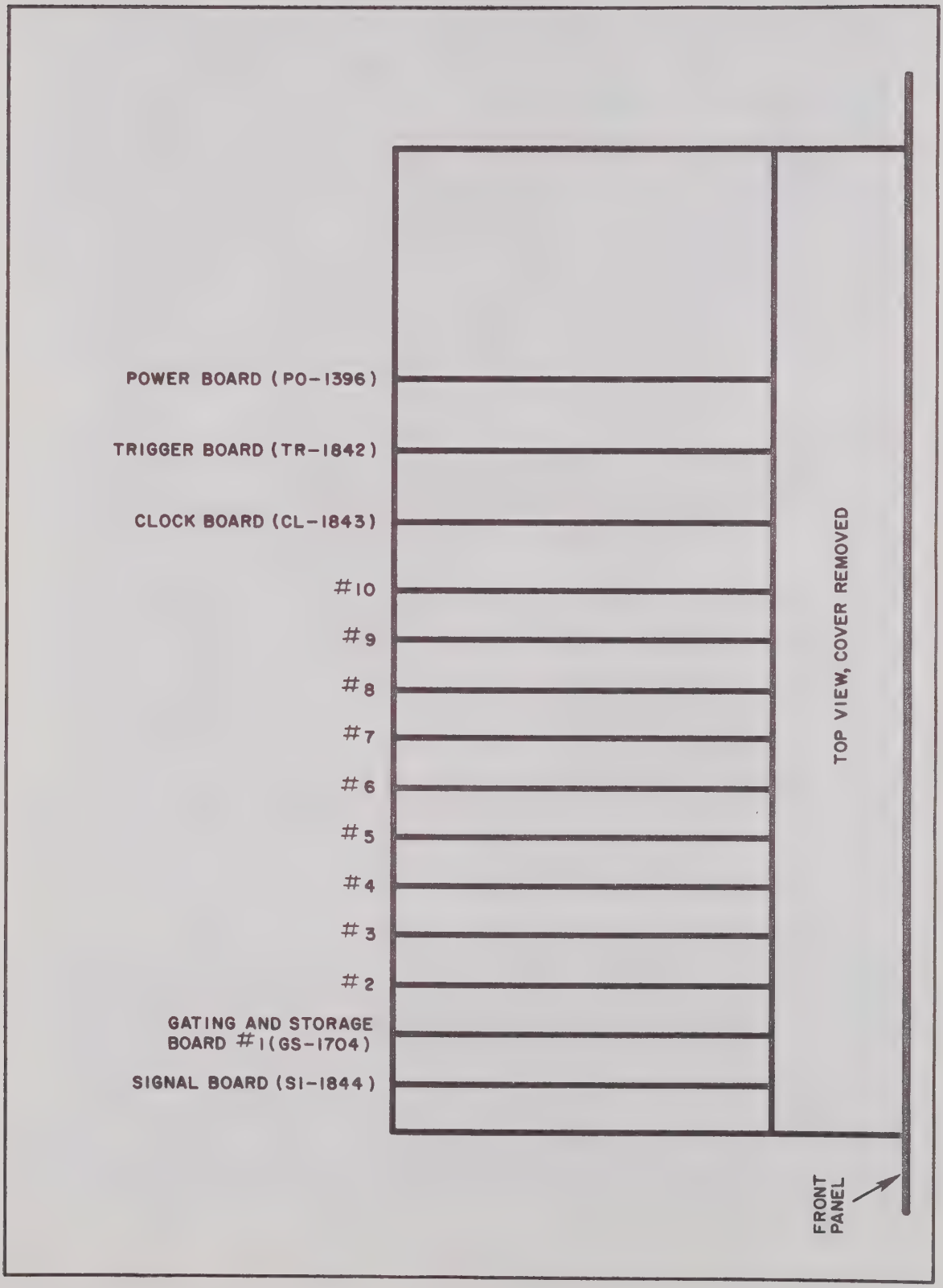

Figure IV-6. LOCATION OF CIRCUIT BOARDS

The second control, R403, shifts the input of Q402 such that "zero in gives zero out". Two facts necessitate this control. The first is that Q400 and Q402 have different emitter-base junction characteristics, and the second is that they are running at considerably different current levels.

AMPLIFIER A2

A2, the second Signal Input Channel Amplifier, is another complementary emitter follower. Its function is to accept the signal from the vernier portion of the Gain Control and supply it at a constant one thousand ohm impedance to the prefilter. With the exception of a few component values, A2 and A1 are identical, and the circuit description of A1 may be considered to apply equally to both amplifiers.

AMPLIFIER A3

The prefilter is followed by A3, a non-inverting operational amplifier with a closed loop gain of 2½. Besides driving the resistive portion of the Characteristic Time Constant Filter, A3 also drives the input of the Overload Detect Circuit. In addition, DC from the "ZERO" Control is supplied to the summing point of A3 to effect zeroing. Basically, A3 consists of two differential pairs followed by an output emitter follower. Transistors Q406 and Q407 constitute the first pair, Q409 and Q410 the second, and Q412 is the output stage. The remaining two transistors, Q408 and Q411, act as constant current sources. The gain determining feedback loop consists of R434, R427, and R433, which shunts R427. Similar to the case of the first two amplifiers, and adjustable current source (R421 and R422) provides the input transistor base current and assures that DC variations will not accompany changes in the prefilter time constant. Feed forward capacitors, C405, and C406, extend the frequency response.

OVERLOAD DETECT CIRCUIT

The Overload Detect Circuit turns on the front panel "OVERLOAD" Light whenever the output of A3 exceeds plus or minus twelve volts. This light is in the collector circuit of Q415, which in turn is driven by Q413, such that whenever Q413 turns on, Q415 goes on and the bulb lights. When the output of A3 is between plus and minus twelve volts, Q414 is biased on and Q413 is biased off. Should the A3 output go more positive than plus twelve volts, Q413 will be turned on through D400, Q415 will go on, and the bulb will light. Should the A3 output go more negative than minus twelve volts, the current through Q414 will increase as D401 becomes forward biased, Q413 will turn on, as will Q415, and the bulb will light. The one microfarad capacitor from the collector of Q415 to the base circuit of Q413 provides positive feedback and assures that even overload transients will solidly light the "OVERLOAD" Light. Furthermore, the capacitor will cause the light to be held on for approximately half a second. In effect, the circuit is a complementary monostable.

AMPLIFIER A4

During each sweep, the memory contents are sequentially applied to A4, the high impedance input amplifier of the Signal Output Channel. In essence, A4 consists of a high input impedance field effect transistor source follower

(Q419), followed by two emitter followers (Q421 and Q422), a gain of four common base stage (Q423) and an output emitter follower (Q425). Field effect transistors Q417 and Q418 act as "crowbars", and short the amplifier input to ground whenever a sweep is not occurring. Note that the crowbar control signal (CR IN) is supplied not only to the crowbar transistor gates, but also to inverter Q416, and that a portion of the inverted signal is coupled through the "FLAT LINE COMPENSATOR" capacitor, C416, to the gate of Q419, allowing neutralization of the crowbar transistor switching transients. Q420 is a constant current source for Q419. The trimpot in the bias circuit of Q420 acts as a zero adjust for A4. Of the two transistors not yet mentioned. Q426 is a constant current source for Q425, and Q424 establishes the base potential of common base stage Q423. Neutralization of the Signal Bus stray capacity is effected by the adjustable RC combination C412, C414, and R469.

AMPLIFIERS A5 AND A6

Following amplification by A4, a signal will be applied either directly to A6 (no smoothing), or, if the operator has elected to insert smoothing, indirectly through the first section of the smoothing filter to A5. The output of A5 then drives the second section of the smoothing filter, the output of which in turn is applied to A6. A5 acts as a buffer between the two sections of the smoothing filter. A6 acts as a buffer between all preceding circuitry and the output jacks. Both A5 and A6 are similar to A1, and the circuit description of that amplifier applies to them as well. Note that A6 has two outputs. The "7 k" output is supplied through the 15 k Recorder Sensitivity Control to the output binding posts. The 600 ohm output goes directly to the front panel "OUT" Jack.

GRD AND PRE-GRD

Note that the Signal Amplifier Board is referenced to two separate grounds, "PRE-GRD" and "CHASSIS GRD". Those circuits belonging to the "PRE-GRD" System are referenced to the front panel Signal "IN" Jack. Those circuits belonging to the "CHASIS GRD" System are referenced to the chassis. The front panel "IN" Jack is mounted directly on the front panel, thereby maintaining continuity between the two ground systems. Dividing the grounds into two separate systems assures that no degradation or oscillation will occur because of high level or transient signals finding their way into the Signal Input Channel by way of ground loops.

4.9 TRIGGER BOARD

Located on the Trigger Board are a Schmitt Trigger, which allows synchronization with a wide range of external trigger waveforms, the Delay Monostable, the Gate Generator and Ready Light Circuit, and some power supplies which produce the DC levels required by the ring counter. The rectifier bridge which provides the plus and minus unregulated DC to the plus and minus twenty-four volt power supply board is also located on the Trigger Board.

SCHMITT TRIGGER

Observing the Schmitt Trigger portion of the Trigger Board Schematic (page VIII-6), note that the trigger level is determined by the "THRESHOLD" Control,

R33. Whenever the input waveform reaches that amplitude necessary to overcome the threshold current through R201, the Schmitt will fire. R207 provides the positive feedback to realize a good "snap". Emitter followers Q201 and Q204 provide isolation from the "external world" and reference respectively, while Q205 and Q206 provide sharp trigger pulses to following stages. Because the circuits which follow the Schmitt Trigger require positive trigger pulses, two Schmitt outputs are provided to allow external triggering of the TDH-9 from either the plus or minus slope of an applied trigger waveform. With the Slope Switch in the "+" position, the "SCHMITT +" output will be a positive pulse when the positive slope of the trigger waveform crosses over the threshold level, and this "SCHMITT +" output will be routed through the Slope Switch to the following circuits. With the Slope Switch in the "-" position the "SCHMITT -" output will be a positive pulse when the negative slope of the trigger waveform crosses the threshold, and this "SCHMITT -" output will be supplied to the following circuits.

DELAY MONOSTABLE

The next trigger board circuit is the complementary type Delay Monostable, which comprises transistors Q207 through Q213 and their associated components. Considering the functions of the different transistors, Q207 is the quiescently-off input stage. Q208 acts both as the output and as a drive for Q209, which in turn drives the Monostable Capacitor. Current control is provided by Q211 and indirectly by Q210, the emitter current of which is determined by the front panel "duodial" Delay Control. The Monostable Capacitor, through emitter follower Q212, controls Q213, the output of which is fed back to the input stage.

Consider the circuit operation beginning with the quiescent state. Q211 conducts according to the setting of the duodial. This current is constant whether the monostable is active or not. The drop of forward biased D211 establishes the collector potential of Q211 at +0.6 volts. The drop across R234 establishes the emitter voltage of Q212 at +0.6 volts, and that transistor will be off. Q213 is biased on through R234. Because Q213 is on, Q207 is reverse biased. Consequently the base of emitter follower Q208 will be at plus six volts, "MONO OUT" will be at five volts, and the emitter of Q209 will follow. Assume a positive transient is applied to C205. D206, which passes only positive pulses, will couple the pulse to the base of Q207 and turn it on. Its collector will go to ground, Q208 and Q209 will follow, and the negative excursion will be coupled through the Monostable Capacitor, turning off D211. Q212 follows and Q213 will be turned off. Because the output of Q213 feeds back to Q207, the latter transistor will remain on until Q213 is turned back on, and this will not happen until the constant current supplied by Q211 "fills" the Monostable Capacitor sufficiently to again bring the base potential of Q212 above ground, thereby forward biasing the emitter base junction of Q213. During the monostable active time, "MONO OUT" will be approximately minus one volt. The recovery time of the monostable, determined by the output impedance of Q209, the Monostable Capacitor, and resistor R233, is about seven percent of the delay time. Delay jitter is typically .01% of the delay time.

GATE GENERATOR AND READY LIGHT

Also located on the Trigger Board are the Gate Generator and Ready Light Drive

Circuit. Whenever a sweep begins, Q214 will turn off, biasing Q215 on and Q216 off. The Ready Light will go out and the collector potential of Q215 goes to within one percent of five volts. These conditions prevail until the sweep is completed, at which time the "GATE IN" goes negative, the "READY" Light goes out, and the "GATE OUT" level returns to ground potential.

TRIGGER BOARD POWER SUPPLY CIRCUITS

Two blocks of power supply circuits are located on the Trigger Board. The first is the bridge (D200 through D203) which furnishes unregulated plus and minus 31 volts to the power supply board. The second comprises a series of emitter follower type regulators which establish reference levels for the ring counter. Both are straightforward and require no detailed descriptions.

4.10 CLOCK BOARD

Clock Board Circuits include the Clock Oscillator Control Gate, the oscillator itself, the two logic ring stages, OOA and OOB, the Bistable, and the Ramp Generator.

CLOCK OSCILLATOR

Transistors Q303 through Q311, together with their associated components, constitute the Clock Oscillator. In essence, the clock is a triangular wave oscillator, the frequency of which is a function of the amplitude and slope of the triangular waveform. The slope in turn depends on the ramping rate of a capacitor, which is being "filled" from a constant current source. Changing sweep time ranges causes different valued ramping capacitors to be switched in. Adjusting the large Sweep Time Duration Control changes the magnitude of the constant ramping current. The two together permit selection of oscillator frequencies from 1 MHz to 1 Hz (the latter frequency being fixed). These frequencies correspond to sweep times of 100 microseconds and 100 seconds respectively. Q304 and Q305 are control transistors. Q306 is a current inverter. Transistors Q307 through Q310 constitute a Schmitt Trigger, which, by "firing" whenever the "triangles" reach plus three volts or +0.3 volts, periodically causes reversal of the ramping current, thereby achieving true triangular waves. Q311 is the output emitter follower.

Q303, the constant current source, always makes current available to the control transistors Q304, Q305, and to the current inverter, Q306. Quiescently, Q304 is biased on and Q305 off. The current from Q303 flows through Q304 and biases Q306 on. Because R309 and R310 are equal, and because D304 compensates the emitter base drop of Q306, the collector current of Q306 equals that supplied by Q303, though of opposite direction. Forward biased D306 establishes the potential at the junction of D306, R317, and the Clock Capacitor at minus 0.6 volts. Because the base of Q310 is biased at plus three volts and the base of Q307 is at -0.6 volts, Q308 is off, Q309 on, and the "CLOCK OUT" potential at R326 is plus 3.5 volts.

Starting of the oscillator is effected when the Run Gate senses a command to begin a sweep, and biases Q304 off, and, consequently, Q305 on and Q306 off. The current now being supplied to the Clock Capacitor is of opposite direction to the quiescent state current, and the potential across the capacitor begins

rising linearly (D306 is immediately biased off) at a rate of i/C volts per second, where "C" is the Clock Capacitor and "i" is the current supplied by Q303. This linear rise in voltage continues until the Schmitt Trigger fires, which will occur when the ramp reaches about plus three volts. The "CLOCK OUT" point follows the change of state of the Schmitt Trigger by going immediately to +0.5 volts. At the same time, because of the feedback from the collector of Q309 to the base of Q305, the control transistors switch; Q305 goes off, Q304 comes on, and the direction of the current being supplied to the Clock Capacitor is reversed. The positive linear rise in voltage across the Clock Capacitor also reverses. Because the change in ramping current was only one of direction and not magnitude, the ramp slope simply changes sign. This linear decrease in voltage continues until it reaches approximately +0.3 volts, at which time the Schmitt fires again. The accompanying reverse in ramp current direction and slope sign marks the end of the first complete cycle. For all subsequent cycles except the last, the voltage swing of the ramp will be between plus three and +0.3 volts. When the logic senses that ring stage 00A has just come on, marking the end of one sweep, the Run Gate turns Q304 sufficiently hard on so as to prevent Q305 from being turned on again when the Schmitt fires for the last time. The ramp continues on down until "caught" by D306 at minus 0.6 volts; the quiescent state is restored.

The Clock Oscillator output is a positive three-volt square wave, referenced to +0.5 volts. The negative going edge of the square wave marks the crossover from positive to negative ramp slope, or simply the triangle peaks. Because of the time required for the ramp to rise from minus 0.6 volts to plus three volts, an inherent delay of about 0.6% of the sweep time will be inserted between the trigger command time and the beginning of the sweep. This delay is independent of and in addition to any monostable delay.

CLOCK BOARD GATES

The three logic gates, "DON'T RUN", "RUN", and "TRIGGER", are located on the clock board. Because the functions of these gates were treated in some detail under "CONTROL LOGIC", the emphasis in this discussion will be on how they effect their control.

(1) RUN GATE

The "RUN" Gate, which comprises transistors Q300 through Q302 and their associated components, directly controls Q304 and thereby the Clock Oscillator. In the quiescent state, Q301 will be on, and, consequently, so will Q304. Anytime that Q301 goes off, control of Q304 and Q305 goes over to the Clock Schmitt and the oscillator commences to oscillate. Note that the "RUN" Gate has two inputs, the first being at the base of Q300 and the second being the anode of D302. If either one of them goes sufficiently positive to pull the emitter of Q301 above ground potential, that transistor will shut off and the clock will start. Once started, it will continue oscillating until both run gate inputs are down (or open as the case may be for the number two input), which can occur only when the sweep is completed and ring stage 00A is on again. Q302 drives the inhibit input of the Trigger Gate.

(2) DON'T RUN GATE

The cathodes of diodes D300 and D301 are the two inputs of the "DON'T RUN" Gate, which directly controls input number one of the "RUN" Gate. Logically, the "DON'T RUN" Gate is a simple two-channel positive "AND" Gate. Its logical relationship to the other gate and to clock control is covered in some detail under "CONTROL LOGIC" (page IV-8).

(3) TRIGGER GATE

This last gate also has two inputs, one capacitive (C303) and one resistive (R328). Q312, an inverter, is normally biased off. If a positive going trigger input is applied to C303, Q312 will be momentarily forward biased and will drive the base of Q313 with a negative pulse to advance the ring counter. Negative going inputs will simply drive Q312 further into cutoff and will be ignored. However, whenever the "RUN" Gate is allowing the clock to oscillate, Q302 will be off and Q312 will be biased so far into cutoff through R308 and R328 that a trigger command applied to C303 will not be able to pulse Q312 on and will consequently be ignored, thereby effecting a trigger inhibit action whenever a sweep is in progress.

LOGIC RING STAGES

Two ring stages, 00A and 00B, are also located on the Clock Board. Each stage of the ring counter has two transistors except these two logic stages, which have an emitter follower output as well. Observing the schematic (page VIII-5), note that 00A and 00B are alike except that 00A has a 5.6 k resistor (R336) which gives it a slight turn on preference, assuring that whenever the instrument is turned on, 00A will be the quiescently on stage. Because R334 acts as the emitter resistor for all 102 stages of the ring counter, and because of the references provided by the minus seven and minus nine volt power supplies, only one stage can be on at a time. All others will be off.

Consider the quiescent state. Q315 and Q316 will be on and the emitter bus will be at about minus 7.5 volts. To begin a sweep, a negative pulse is applied to the emitter bus by way of the emitter bus drive transistor, Q313. This negative pulse turns 00A momentarily off. As Q316 goes off, its collector voltage rises sharply and Q317 follows. This positive pulse is applied through C306 to the base of Q319, and, because the time constant is longer than the duration of the emitter bus drive pulse, 00B comes on, advancing the ring counter one step. The counter continues to advance in like manner until 00A comes on again (Q312 is the buffer between stage 100 and 00A), restoring the quiescent state.

BISTABLE

Transistors Q321 and Q322, along with their related components, constitute the bistable discussed under "RAMP AND GATE OUTPUTS" (page IV-8). Because the circuit is conventional and its operation straightforward, no description other than that already presented under "RAMP AND GATE OUTPUTS" is provided.

RAMP GENERATOR

The Ramp Generator, transistors Q324 through Q331, is divided into two sections. The first is the 00A ring stage controlled constant current source (Q324 and Q325), and the second is the operational amplifier (Q326 through Q331), the output of which is capacitively fed back to the input by way of the Ramp Capactior to form an integrating-type ramp generator. In the quiescent state, 00A is on, its output is down, and Q324 is biased off through D316. Because Q325 will also be off, no current will be available to fill the Ramp Capacitor, and no ramping can occur. The first trigger pulse advances the ring counter from 00A to 00B, unlocking D316 and making ramping current available. Note however, that as soon as 00B comes on, Q326 is biased on, shorting out the "RAMP CAPACITOR". The ramp generator output will remain at ground potential until, when 00B goes off, actual sequencing of the memory-control ring stages begins. At that time, the current, made available when 00A went off, will begin filling the Ramp Capacitor, and the ramp generator output voltage will begin rising linearly. It will continue to rise until 00A comes on again, marking the end of the Sweep, at which time it will "hold" at its final value. The ramp slope is determined by the size of the Ramp Capacitor and the magnitude of the ramping current. The former is a function of the sweep range and the latter a function of the sweep vernier control setting. Two calibration trimpots are provided, R356, the ramping current calibrator, and R371, which establishes the reset level at zero volts.

4.11 GATING AND STORAGE BOARD

There are ten Gating and Storage Boards, on each of which are mounted ten memory-control ring stages along with the corresponding gates and memory capacitors. Observing the schematic (page VIII-4), note that these ring stages are similar to the already described 00A and 00B, except that the latter havee emitter follower outputs.

Each memory control ring stage drives an MOS type field-effect transistor gate, each of which has its drain in series with the corresponding memory capacitor (through a 100 ohm resistor). The source of each gate transistor is returned to the Signal Bus. For the time that each ring stage is on, the corresponding gate opens, allowing change or "correction" in the magnitude of the charge stored on the corresponding memory capacitor. Associated with each gate are a 100 ohm resistor and a 9-35 picofarad trim-capacitor, which permit equalization of the field effect transistor capacity from one stage to the next. When capacity equalization is realized, the internal "noise" will be at a minimum. It might be pointed out that both this "noise" and the effect of adjusting the trim-capacitors are noticeable only at the faster sweep times.

4.12 POWER SUPPLY BOARD

The regulator circuitry of the plus and minus twenty-four volt power supplies is located on the Power Supply Board. Because these regulators are completely conventional, no detailed description is furnished.

4.13 ODDS AND ENDS BOARD

Besides the fourteen "plug-in" boards, there is a fifteenth "wired-in" board, which is permanently mounted on the back of the front panel. Observing the Chassis Wiring Schematic (page VIII-8), note that many of the TDH-9 timing and filter capacitors are located on this board. Also located there is a bistable which acts as a buffer between the Manual Trigger Pushbutton Switch and the following circuitry. Use of a bistable here eliminates any problems which might result from contact bounce of the pushbutton switch.

SECTION V
CALIBRATION

5.1 INTRODUCTION

Owing to component aging, it may be necessary to periodically align the TDH-9 if the highest confidence in experimental data obtained with the instrument is to be maintained. In general, alignment should be carried out after each 3000 hours of operation. However, unusually harsh environmental conditions could require that the alignment be performed earlier.

The TDH-9 alignment comprises five major divisions. They are the Power Supply Calibration, Timing Adjustments, DC Alignment, Low Frequency Alignment, and the High Frequency Alignment. With the exception of the Power Supply Calibration, each of these constitutes a separate procedure in itself, which can be carried out independent of the others. Because any change in the highly regulated plus and minus twenty-four volt levels affects all phases of instrument performance, it is essential that the power supply be properly aligned before proceeding with any of the other separate alignment procedures.

The location of all potentiometers and variable capacitors, together with the test points, is indicated in Figure V-1.

5.2 EQUIPMENT NEEDED

(1) Extender Board, PAR #EB 1337/TDH-9.

(2) Oscilloscope, DC to 1 MHz, 10 millivolts/cm. sensitivity, differential input with a common mode rejection ratio of 1000:1 or better.
Suggested Instrument: TEKTRONIX Type 502A or equivalent.

(3) DC voltmeter, input impedance of 1 Megohm or higher, 0.5% accurate at five volts and 24 volts.
Suggested Instrument: NLS Type X-2 or equivalent.

(4) Frequency/Period Counter, 1 Hz to 100 kHz, three volt sensitivity.
Suggested Instrument: HEWLETT PACKARD Type 5212A or equivalent.

(5) Signal Generator, 50 Hz to 500 kHz.
Suggested Instrument: HEWLETT PACKARD Type 200 CD or equivalent.

(6) Attenuator, 10:1, 0.1% accurate when loaded with 100 k ohms.

(7) Alignment Screwdriver.

(8) Six inch clip lead.

5.3 PRELIMINARY CONSIDERATIONS

(1) Turn the power off.

(2) Remove the top and bottom covers of the instrument.

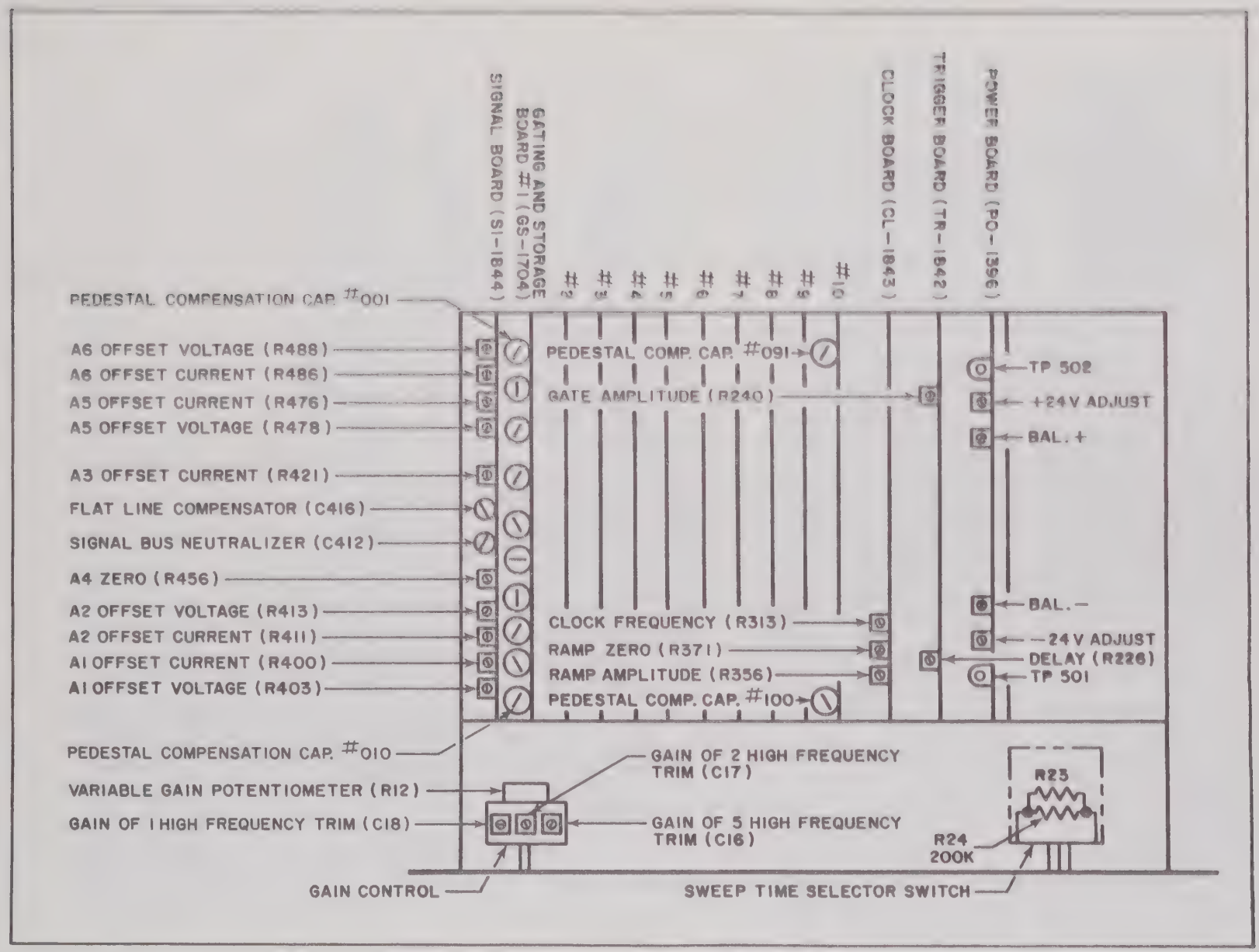

Figure V-1. ADJUSTMENTS AND TEST POINTS

(3) Remove the 14 plug-in printed circuit boards, taking care to note the order of the ten Gating and Storage Boards so that each can be returned later to its proper connector. These boards are numbered (upper corner) to facilitate keeping them in order. NOTE: Although the Gating and Storage Boards are interchangeable, changing their order will "throw off" the original alignment and unnecessarily prolong the realignment.

(4) All measurements are with respect to chassis ground unless otherwise noted.

5.4 POWER SUPPLY CALIBRATION

(1) Insert the Power Supply Board (PO 1396) into the Extender Board (EB 1337/TDH-9).

(2) Insert the Extender Board (with the Power Supply Board attached) into the power supply board chassis connector.

(3) Turn the power on.

(4) Monitor TP 501 (Power Supply Board) with the DC voltmeter.

(5) Adjust "-24 ADJ" until the meter indicates -24 volts.

(6) Short the bases of Q505. NOTE: Q505 is one of two glued pairs located on the Power Supply Board. To determine which are the base leads, check the Power Supply Board Schematic, page VIII-8.

(7) Adjust "BAL-" until the meter indicates -24 volts, or until the adjustment becomes such that a slight adjustment of the trimpot causes the reading to swing from minus three to minus thirty-two volts or vice versa.

(8) Remove the short and ascertain that the voltage is still -24 volts.

(9) Monitor TP 502 with the DC voltmeter.

(10) Adjust "+24 ADJ" until the meter indicates +24 volts.

(11) Short the bases of Q510, the other glued pair.

(12) Adjust "BAL +" until the meter indicates +24 volts, or until the adjustment becomes such that a slight adjustment of the trimpot causes the reading to change sharply from plus three to plus thirty-two volts or vice versa.

(13) Remove the jumper and ascertain that the voltage is still +24 volts.

(14) Remove the Extender Board, separate the Power Supply Board from it, insert the Power Supply Board into its connector.

5.5 TIMING ADJUSTMENTS

CLOCK

(1) Set the TDH-9 front panel controls as follows:

Trigger Mode ---------- INT.
Delay ---------- MIN. DELAY
Sweep Duration ---------- 1, X10 mS

(2) Insert the Trigger (TR 1842), Clock (CL 1843), and the ten Gating and Storage (GS 1704) Boards into the corresponding chassis connectors.

(3) After setting up the counter to measure 10 kHz with the greatest possible accuracy, connect its input to pin R of the TDH-9 rear panel Interface Connector. The signal at pin R is the Clock Output, a +3.5 volt square wave referenced to +0.3 volt.

(4) Adjust the Clock Frequency Trimpot (R313, Clock Board) for an indicated frequency of 10 kHz, making the adjustment as accurate as the resolution of the trimpot permits.

(5) Check the 1, 2, 5, and 11 settings of the five variable (fastest) sweep ranges. Assuming that the counter in use is that designated or its equivalent, it will be convenient at the fastest sweep times to measure the frequency of the Gate Output (available at pin K of the Interface Connector) instead of the clock frequency. Similarly, with the longest sweep times, it is more convenient to measure the period of the clock, rather than its frequency. Table V-1 indicates for which sweep times it is convenient to monitor the gate and clock outputs respectively, whether frequency period is to be measured, and finally, the tolerance limits in each case. Should a somewhat more versatile counter be available, it may be more convenient to simply measure the clock frequency directly on all ranges, in which case the applicable formula is:

$$\underset{(Hz)}{\text{FREQUENCY AT PIN R}} = \frac{100}{\text{SWEEP DURATION (Sec.)}} \pm 5\%$$

(6) Set the front panel Sweep Selector Control to "100 SEC. FIXED SWEEP".

(7) Check that the clock period (pin R) is 1.00 second, plus or minus five percent. If out of tolerance, change the value of R23, which is located across the 200 k metal film resistor mounted on the rear wafer of the Sweep Time Selector Switch. Reducing R23 will shorten the period and increasing it will lengthen the period.

(8) Remove the Counter.

RAMP

(1) Set the TDH-9 front panel controls as follows:

SWEEP DURATION	MEASURE	PIN	LOWER LIMIT	UPPER LIMIT
11, X1 SEC.	PERIOD	R (Clock)	104.5 mS	115.5 mS
5, X1 SEC.	PERIOD	R (Clock)	47.5 mS	52.5 mS
2, X1 SEC.	PERIOD	R (Clock)	19.0 mS	21.0 mS
1, X1 SEC.	PERIOD	R (Clock)	9.50 mS	10.5 mS
11, X100 mS	PERIOD	R (Clock)	10.45 mS	11.55 mS
5, X100 mS	PERIOD	R (Clock)	4.75 mS	5.25 mS
2, X100 mS	PERIOD	R (Clock)	1.90 mS	2.10 mS
1, X100 mS	PERIOD	R (Clock)	.950 mS	1.05 mS
11, X10 mS	FREQUENCY	R (Clock)	864 Hz	954 Hz
5, X10 mS	FREQUENCY	R (Clock)	1.90 kHz	2.10 kHz
2, X10 mS	FREQUENCY	R (Clock)	4.75 kHz	5.25 kHz
1, X10 mS	FREQUENCY	R (Clock)	9.50 kHz	10.50 kHz
11, X1 mS	PERIOD	K (Gate)	10.66 mS	11.78 mS
5, X1 mS	PERIOD	K (Gate)	4.85 mS	5.36 mS
2, X1 mS	PERIOD	K (Gate)	1.94 mS	2.14 mS
1, X1 mS	PERIOD	K (Gate)	.969 mS	1.07 mS
11, X100 µS	FREQUENCY	K (Gate)	848 Hz	937 Hz
5, X100 µS	FREQUENCY	K (Gate)	1.86 kHz	2.06 kHz
2, X100 µS	FREQUENCY	K (Gate)	4.66 kHz	5.15 kHz
1, X100 µS	FREQUENCY	K (Gate)	9.31 kHz	10.29 kHz

Table V-1. TABLE OF SWEEP CALIBRATION CONTROL SETTINGS AND TOLERANCES

Signal Mode ---------- READOUT ONLY
Trigger Mode ---------- MANUAL
Sweep ---------- 10, X100 mS

(2) Observe the Ready Light and check that the manual Trigger Pushbutton Switch must be depressed twice to trigger a sweep.

(3) After a sweep is completed, push the Manual Trigger Pushbutton Switch once.

(4) Connect the DC voltmeter to the "RAMP OUT" Jack.

(5) Adjust the Ramp Zero Trimpot (R371, Clock Board) for an indication of zero volts on the meter.

(6) Depress the Manual Trigger Switch a second time to initiate a sweep and allow the sweep to finish.

(7) The meter should indicate 5.0 volts. If it does not, make a slight adjustment of the Ramp Amplitude Trimpot (R356, Clock Board). NOTE: Adjusting the pot does not change the amplitude of the just completed ramp (the meter reading), but instead determines the amplitude of subsequent ramps (the meter reading after initiating another sweep).

(8) Initiate another sweep and again check the final ramp amplitude. If necessary, adjust R356 again to obtain a final ramp amplitude of 5.0 volts.

(9) Set the front panel Sweep Selector Control to "100 SEC FIXED SWEEP".

(10) Start a sweep and allow it to finish (100 seconds).

(11) The voltmeter should indicate 5.0 volts. If it does not, it will be necessary to change the value of R362, a fixed resistor located on the Clock Board (See Schematic, page VIII-5). Increasing the value of R362 will reduce the final ramp voltage, decreasing the value of R362 will increase the final ramp voltage. In general, a 500 k ohm change in the value of R362 will change the ramp amplitude 1%.

(12) Remove the voltmeter.

DELAY

(1) Set the TDH-9 front panel controls as follows:

Trigger Mode ---------- INT
Delay ---------- 1, X10 mS
Sweep ---------- 1, X1 mS

(2) Set up the counter to measure period and connect its input to pin K of the TDH-9 rear-panel Interface Connector, where the positive five volt, zero-referenced Gate Output is available.

(3) Adjust the Delay Trimpot (R226, Trigger Board) for an indicated period of 11.0 mS, plus or minus .1 mS, taking care that the counter is indicating the total period and not just the delay or sweep interval.

(4) Monitor the front panel "GATE OUT" Jack with the oscilloscope, which should be triggered by the trailing edge of the Gate Signal to allow easy measurement of the Delay.

(5) Using the oscilloscope, check the 1, 2, 5, and 11 settings of each delay range for ten percent accuracy. Adjust the sweep time controls as necessary to maintain the Delay to Sweep Time Ratio at 10:1. For delays less than one millisecond, set the sweep controls for "1", "X100 μS".

(6) Remove the Oscilloscope and the Counter.

GATE AMPLITUDE

(1) Set the TDH-9 front panel controls as follows:

Delay ---------- MIN. DELAY
Sweep Duration ---------- 100 SEC. FIXED SWEEP

(2) Connect the DC voltmeter to the "GATE OUT" Jack.

(3) Adjust the Gate Amplitude Trimpot (R240, Trigger Board) for a meter indication of five volts, plus or minus fifty millivolts. NOTE: At the end of each 100 seconds (the sweep time), the gate voltage will return to zero for two seconds.

(4) Remove the meter.

5.6 DC ALIGNMENT

SIGNAL INPUT CHANNEL

(1) Set the front panel controls as follows:

Input Coupling ---------- DC
Gain Selector ---------- 10
Gain Variable ---------- Fully CCW
Signal Mode ---------- ERASE
Trigger Mode ---------- MANUAL
Sweep Duration ---------- 11, X100 SEC. FIXED SWEEP

(2) Set the rear panel Smoothing Control to "OFF".

(3) Insert the Signal Board (SI 1844) into the Extender Board.

(4) Insert the Extender Board (with the Signal Board attached) into the Signal Board chassis connector.

(5) Attach a clip lead across pins 1 and 4 of the exposed extender board connector.

(6) Connect the voltmeter to pin 5 of the Extender Board. NOTE: Alternatively, one might use the oscilloscope as a voltmeter for the DC alignment.

(7) Adjust the A1 Offset Voltage Trimpot (R403, Signal Board) for a meter indication of zero volts, plus or minus one millivolt.

(8) Remove the clip lead, and adjust the A1 Offset Current Trimpot (R400, Signal Board) for zero volts, plus or minus one millivolt.

(9) Attach the clip lead across pins 4 and 7.

(10) Remove the meter from pin 5 and connect it to pin 6.

(11) Adjust the A2 Offset Voltage Trimpot (R413, Signal Board) for zero volts, plus or minus one millivolt.

(12) Remove the clip lead and adjust the A2 Offset Current Trimpot (R411, Signal Board) for zero volts, plus or minus one millivolt.

(13) Attach the clip lead across pins 6 and 8.

(14) Remove the meter from pin 6 and connect it to pin 14.

(15) Adjust the front panel Zero Control for zero volts, plus or minus .1 volt.

(16) Adjust the A3 Offset Current Trimpot (R421, Signal Board) such that when the clip lead joining pins 6 and 8 is alternately removed and reattached, the DC voltage shift indicated by the meter will be less than one millivolt.

(17) Remove the clip lead and the meter.

SIGNAL OUTPUT CHANNEL

(1) Connect the meter to pin 9 of the exposed extender board connector.

(2) Adjust the A4 Zero Trimpot (R456, Signal Board) for a meter indication of zero volts, plus or minus 100 millivolts.

(3) Attach the clip lead across pins 17 and 23.

(4) Remove the meter from pin 9 and connect it to pin 18.

(5) Adjust the A5 Offset Voltage Trimpot (R478, Signal Board) for zero volts, plus or minus one millivolt.

(6) Remove the clip lead from across pins 17 and 23 and attach it across pins 12 and 23.

(7) Adjust the A5 Offset Current Trimpot (R476, Signal Board) for zero volts, plus or minus one millivolt.

(8) Remove the meter from pin 18 and connect it to pin 19.

(9) Adjust the A6 Offset Voltage Trimpot (R488, Signal Board) for zero volts, plus or minus one millivolt.

(10) Set the rear panel Smoothing Control to "ON".

(11) Adjust the A6 Offset Current Trimpot (R486, Signal Board) for zero volts, plus or minus one millivolt.

(12) Remove the clip lead and the meter.

(13) Remove the Extender Board, separate the Signal Board from it, and insert the Signal Board into its connector.

5.7 LOW FREQUENCY ALIGNMENT

GATE LEAKAGE, POSITIVE

(1) Remove the Signal Board, carefully note the tab position of the two socketed transistors, and remove them.

(2) Replace the Signal Board.

(3) Set the front panel controls as follows:

Signal Mode	ANALYZE AND READOUT
Characteristic Time Constant	5 SEC.
Trigger Mode	INT.
Delay Duration	MIN. DELAY
Sweep Duration	1, X100 mS

(4) Set the Rear Panel Smoothing Control to "OFF".

(5) Connect the oscilloscope to the "SIGNAL OUT" Jack. The scope should be triggered from the leading edge of the Gate Output, which is available at the "GATE" Jack.

(6) Using the oscilloscope as a voltmeter. Ascertain that the TDH-9 Zero Control can swing the voltage at the "SIGNAL OUT" Jack approximately plus and minus ten volts.

(7) Turn the Zero Control fully clockwise.

(8) After two minutes, set the front panel controls, in order, as follows:

Trigger Mode	EXT. (sweeping will stop)
Zero	fully counter-clockwise

(9) After ten minutes, set the front panel controls, in order, as follows:

Signal Mode	READOUT ONLY
Trigger Mode	INT. (sweeping will resume)

(10) Check that the DC level of the pedestals observed at the "SIGNAL OUT" Jack is approximately plus ten volts.

(11) AC couple the oscilloscope and expand the sensitivity sufficiently to permit examination of the "spread" in pedestal amplitudes; the "tops" of all pedestals should lie in a fifty millivolt band. Because the observed spread or change in amplitude from one pedestal to the next will increase with time, it is necessary to note quickly (two-three minutes) whether or not any of the pedestals are outside of the spread tolerance, and if they are, to locate those stages of the Gating and Storage Boards which show a leaky gate. An easy way to establish the correspondence between an observed pedestal and its associated ring stage is to place one hand on ground (any jack), and with a finger of the other hand, to go down the line of Pedestal Compensation Trim-Capacitors on each Gating and Storage Board, touching the adjustment screw of each capacitor in turn. As each screw is touched, the amplitude of the corresponding pedestal will drop from plus ten volts toward ground. When the observed drop occurs in a pedestal which was out of tolerance, the offending stage of the Gating and Storage Boards will have been found.

(12) Replace the RN 4004 Field Effect Transistor in any stage which evidenced a leaky gate, i.e., the corresponding pedestal was outside the fifty millivolt limit. NOTE: These are specially selected transistors and should be obtained from PAR.

GATE LEAKAGE, NEGATIVE

(1) Set the front panel controls as follows:

Signal Mode ---------- ANALYZE AND READOUT

(2) After two minutes, set the front panel controls as follows:

Trigger Mode ---------- EXT.
Zero ---------- fully clockwise

(3) After ten minutes, set the front panel controls as follows:

Signal Mode ---------- READOUT ONLY
Trigger Mode ---------- INT.

(4) Using the oscilloscope as a DC voltmeter, ascertain that the amplitude of the pedestals is approximately minus ten volts.

(5) AC couple the oscilloscope and examine the pedestal amplitude spread; all pedestals should be in a band fifty millivolts peak-to-peak.

(6) Should any pedestal not fall in the fifty millivolt band, replace the RN 4004 Field Effect Transistor of that stage of the Gating and Storage Boards which produced the pedestal.

(7) If any field effect transistors were replaced in either the positive or the negative gate leakage procedure, repeat the two procedures in their entirety.

(8) Remove the Signal Board and replace the two socketed transistors which were removed in step one of the positive gate leakage test procedure.

(9) Disconnect the oscilloscope from the "SIGNAL OUT" Jack.

OVERLOAD DETECT

(1) Set the front panel controls as follows:

Input Coupling -------- GROUND
Gain ------------------ 10
Gain, Variable -------- CAL.
Signal Mode ----------- ANALYZE AND READOUT
Sweep Duration -------- 5, X1 mS

(2) Insert the Signal Board into the Extender Board.

(3) Insert the Extender Board (with the Signal Board attached) into the Signal Board chassis connector.

(4) Connect the oscilloscope to pin 14 of the exposed extender board connector.

(5) Adjust the Zero Control for an indication of zero volts on the oscilloscope (DC Coupled).

(6) Select "DC" coupling at the TDH-9 front panel.

(7) Set up the Signal Generator to supply 50 Hz, and connect its output to the "SIGNAL IN" Jack.

(8) Adjust the signal generator output amplitude such that the observed signal at pin 14 is twenty volts, peak-to-peak.

(9) Using the TDH-9 Zero Control to change the DC level of the signal being observed at pin 14, check that the overload light flashes whenever the signal crosses either +11.5 to +12.5 volts, or -11.5 to -12.5 volts.

(10) Disconnect the Oscilloscope from pin 14 of the Signal Board.

MEMORY GATE RESISTANCE

(1) Connect the oscilloscope to the "SIGNAL OUT" Jack.

(2) Adjust the TDH-9 Zero Control until the DC component of the output signal is zero volts.

(3) Trigger the oscilloscope with the TDH-9 Gate Output. The oscilloscope sweep time should be .5 mSec/cm.

(4) Check that all pedestals are less than three volts peak-to-peak. Should any pedestals be found which are out of tolerance, replace the RN 4004 gate of that stage of the Gating and Storage Boards which produced that pedestal. NOTE: Because the signal being applied to the "SIGNAL IN" Jack is non-synchronous with respect to the sweep, each pedestal will be moving both positive and negative at a high rate, and consequently, will appear to be bi-polar with a clearly defined positive and negative plateau. At the same time the "positive plateau trace" and the "negative plateau trace" will appear to be increasing and decreasing in amplitude at a rate determined by the relationship between the oscilloscope sweep rate and the frequency of the non-synchronous sine wave. Because the oscilloscope sweep time is fixed, by making slight corrections in the frequency of the input signal, it will be possible to make this rate of change of the pedestal amplitude as slow as one desires, and consequently, very easy to determine if any of the pedestals exceed the three volts peak-to-peak maximum amplitude.

If any gate transistors are replaced, it will be necessary to go back and repeat the positive and negative gate leakage test procedures. Also, these are specially selected transistors and should be obtained from PAR.

CROWBAR RESISTANCE

(1) With the TDH-9 front panel Trigger "MODE" Switch, select "MANUAL".

(2) Observe that the signal amplitude at the "SIGNAL OUT" Jack is less than 150 millivolts, peak-to-peak. Should the signal exceed 150 millivolts, peak-to-peak, replace the two socketed transistors which are located on the Signal Board. NOTE: These are specially selected transistors and should be obtained from PAR.

GAIN

(1) Remove the two socketed transistors on the Signal Board, being careful to note the position of the locating tabs.

(2) Insert the 10:1 0.1% accurate attenuator between the Signal Generator output and the "SIGNAL IN" Jack.

(3) Connect the oscilloscope differentially between the input of the attenuator and the TDH-9 "SIGNAL OUT" Jack.

(4) Ascertain that the differential signal is less than 80 millivolts peak-to-peak. If it is greater, change the value of 462 (Signal Board) until the observed signal is less than 80 millivolts peak-to-peak.

(5) If the value of R462 is changed, repeat steps one and two of the Sig-

nal Output Channel Alignment Procedure (page V-8).

(6) Replace the two transistors which were removed in step one of the "GAIN" check.

(7) Disconnect the oscilloscope.

(8) Remove the Extender Board, separate the Signal Board from it, and insert the Signal Board into its connector.

5.8 HIGH FREQUENCY ALIGNMENT

NOTE: Throughout the High Frequency Alignment, all fourteen plug-in printed circuit boards must be installed directly, i.e., without the Extender Board.

INPUT ATTENUATOR COMPENSATION

(1) Set the front panel controls as follows:

Input Coupling --------- AC
Gain ------------------- 10
Gain, Variable --------- CAL.
Trigger Mode ----------- EXT.

(2) Connect the oscilloscope input through a standard 10 Meg. 10:1 probe to the wiper (middle terminal) of the Variable Gain Potentiometer (R12), which is mounted on the rear of the "GAIN" Switch.

(3) Connect the signal generator, the output of which should be one volt peak-to-peak at 1 kHz, to the "SIGNAL IN" Jack.

(4) Ascertain that the observed signal is one volt, peak-to-peak.

(5) Set the TDH-9 gain to "5".

(6) Adjust the signal generator controls for an output signal of two volts peak-to-peak at 500 kHz.

(7) Adjust the Gain-of-5 capacitor (C16, Gain Switch) for an observed signal of one volt peak-to-peak.

(8) Increase the Signal Generator Output to five volts peak-to-peak.

( ) Set the TDH-9 gain to "2".

(10) Adjust the Gain-of-2 capacitor (C17, Gain Switch) for an observed signal of one volt peak-to-peak.

(11) Set the TDH-9 gain to "1".

(12) Increase the Signal Generator Output to ten volts peak-to-peak.

(13) Adjust the Gain-of-1 capacitor (C18, Gain Switch) for an observed signal of one volt peak-to-peak.

(14) Remove the Signal Generator and the Oscilloscope.

PEDESTAL COMPENSATION

(1) Set the rear panel Smoothing Switch to "OFF".

(2) Set the front panel controls as follows:

Input Coupling	GROUND
Gain	10
Signal Mode	ERASE
Characteristic Time Constant	5 SEC.
Trigger Mode	INT.
Delay	1, X100 μS
Sweep Duration	1, X100 μS

(3) Connect the input of the oscilloscope, which should be triggered by the TDH-9 Gate Output, to the "SIGNAL OUT" Jack.

(4) Adjust the Signal Bus Neutralizing Capacitor (C412, Signal Board) for minimum ringing of the observed waveform.

(5) Adjust the Flat Line Compensator (C416, Signal Board) for the best straight line.

(6) Set the front panel controls as follows:

Signal Mode	ANALYZE AND READOUT
Zero	Adjust carefully for zero out (DC couple the scope).

(7) Ascertain that the pedestal scatter is less than 200 mV peak-to-peak. If the scatter is greater than 200 mV peak-to-peak, adjust the 100 Pedestal Compensation Capacitors until the scatter is brought within tolerance. NOTE: Before adjusting the Pedestal Compensation Capacitors, be sure that the Zero Control is adjusted such that the output signal mean value is zero volts; the total positive pedestal area should equal the total negative pedestal area. If the mean value is not zero, as consecutive pedestals are reduced to zero, an error will accumulate which will eventually be beyond the adjustment range of the Compensation Capacitors. A similar effect will be observed if the Flat Line Compensator is out of adjustment.

Once sure that the Zero Control and the Flat Line Compensator are properly adjusted, select a pedestal capacitor at random and adjust it through its full range several times, observing carefully the effect on the output signal. Note that the pedestal corresponding to the selected Compensation Capacitor will move both positive and negative with respect to its initial level, and that the next consecutive pedestal, AND NO OTHER, will change an equal amount in the opposite

direction. This equal and opposite effect is very important because it enables cancellation-compensation of pedestals which are beyond the adjustment range of the corresponding Compensation Capacitor.

For example, suppose that after adjusting a sequence of Compensation Capacitors without difficulty, a pedestal is reached which is too positive to be brought within allowable limits. To bring this pedestal into range, first go back about ten pedestals and set the pedestal reached slightly positive (keeping within allowable limits). The following pedestal (moving toward the problem pedestal), in response to the equal and opposite effect, will become negative to the same degree as the first was adjusted positive. Now adjust this pedestal until it too is slightly positive. The third pedestal will become negative by an amount equal to the sum of the adjustments of the first two; a negative peak is being built up, stage-by-stage. By continuing to adjust each pedestal slightly positive, the negative peak will build up higher and higher. When this negative peak is finally "slid" into the excessively positive pedestal, cancellation will occur, the "problem pedestal" will be brought within the adjustment range, and all of the involved pedestals will be within tolerance. Some practice may be required to gain a feel for distributing offset among several stages to build a peak of proper amplitude.

With these hints as an aid, proceed to adjust the 100 Pedestal Compensation Capacitors in sequence, beginning with 001 and ending with 100.

(8) Connect the output of the signal generator, the controls of which should be adjusted for an output signal of two volts peak-to-peak at 100 kHz, to both the "SIGNAL IN" Jack and the Trigger "IN" Jack.

(9) Set the front panel controls as follows:

Input Coupling --------- AC
Trigger Mode ---------- EXT.
Delay ----------------- MIN. DELAY

(10) Ten cycles of a sine wave should now appear at the oscilloscope during each TDH-9 sweep interval. After this signal has "settled", set the Signal Mode Switch to the "READOUT ONLY" position, and adjust the Signal Bus Neutralizing Capacitor (C412, Signal Board) for slowest distortion or loss of signal.

(11) Set the front panel controls as follows:

Coupling -------------- GROUND
Trigger Mode ---------- INT.
Delay ----------------- 1, X100 μS

(12) Remove the Signal Generator.

(13) Adjust the 100 Pedestal Compensation Capacitors for a pedestal scatter of no more than fifty millivolts peak-to-peak.

(14) Remove the oscilloscope.

SECTION VI
TROUBLESHOOTING

6.1 INTRODUCTION

Featuring conservative design, quality components, and solid state circuitry throughout, the TDH-9 is a precision, highly reliable instrument, and as such, should provide long troublefree service. Component deterioration, however, could incur an occasional malfunction. For this reason, the following paragraphs, which treat possible problems, malfunctions, and their likely causes, have been provided.

Generally, it will be advantageous to use this section in conjunction with Section IV, which deals with the TDH-9 organization and circuitry, and with Section V, which deals with the calibration of the instrument.

6.2 SYMPTOMS, CAUSES AND CHECKS

SYMPTOM 1

Unit inoperative, pilot light out.

CAUSES

(1) AC power not reaching unit.

(2) Line fuse blown.

(3) Power transformer burned out or shorted.

(4) Power supply filter capacitors, C12 and C13, shorted.

(5) Any of the power supply bridge rectifiers, D200, D201, D202, or D203 shorted or open (Trigger Board).

SYMPTOM 2

Does not sweep in any trigger mode.

CAUSE 1

Plus and minus twenty-four volt supply voltages out of tolerance.

CHECK

TP 501 and TP 502 for minus and plus twenty-four volts respectively. If either voltage is low, check for a low impedance short from plus or minus twenty-four volts to ground. Both power supplies are current limited at about 530 milliamperes.

CAUSE 2

Ring supply voltages out of tolerance (± one volt).

CHECK

Trigger Board pins 14, 15, 16, and 18 for minus nine, plus three, minus seven, and minus eleven volts respectively. If any of the voltages are out of tolerance, trouble may be in either the Ring Counter or the ring voltage supplies, which are located on the Trigger Board.

CAUSE 3

Defective Ring Stage.

RING COUNTER TROUBLESHOOTING PROCEDURE

(1) Set the controls for internal triggering, a sweep duration of 100 microseconds, and minimum delay.

(2) With an oscilloscope, examine the signal on the Emitter Bus (pin 21 of the Clock Board). This signal should comprise a continuous series of pulses, spaced one microsecond apart, about 100 nanoseconds wide, and having a peak amplitude of about 300 millivolts. They should be referenced to minus seven volts. If the Emitter Bus is not at minus seven volts, look for a short. If the Emitter Bus is at minus seven volts but the pulse train is missing, check the Clock Oscillator and its associated control circuits.

(3) If the pulse train is as specified, determine which of the 102 ring stages has "hung up" by checking the collector voltage of the 2N3646 in each stage. All but one of these collectors should be plus three volts, indicating that they are off. The 2N3646 collector voltage of the "on" stage will be minus nine volts. NOTE: If stage 00A appears "hung-up", the problem may not be with stage 00A but instead with 00B, which is refusing to come on. For all other stages, "hang up" means that stage, and not the succeeding one, is defective.

(4) Find and replace the defective component of that stage.

(5) Another possibility is that one stage is refusing to come on. When that occurs, the "preferred" 00A stage will come on immediately, with the result that sweeps will be short; only those gates prior to the defective ring stage will be turned on during a sweep. Because stage 100 is never reached under these conditions, the bistable will not change state at the end of each sweep, the Ready Light will not come on, and visible indications will be the same as when the Ring Counter is hung up. If the light does not come on, and an oscilloscope examination of the 2N3646 collectors indicates that the ring is advancing, before assuming that the light or its control circuitry is bad, make sure that each sweep advances through the entire Ring Counter. If subsequent examination shows that there is in fact a defective ring stage, repair that stage.

SYMPTOM 3

Does not sweep, but only with combination of "MIN. DELAY" and "INT." Trigger.

CAUSE

Number two input of the Run Gate is ineffective.

CHECK

R36 (mounted on the Delay Selector Switch) and D302 (Clock Board).

SYMPTOM 4

Does not sweep, but only with combination of "MIN. DELAY" and "EXT." Trigger.

CAUSE

Schmitt Trigger not firing.

CHECK

(1) That the externally supplied trigger pulse has an amplitude of at least 0.5 volts and a width of at least one microsecond.

(2) That the "SLOPE" and "THRESHOLD" are properly set.

(3) The Schmitt Trigger circuit, transistors Q201 through Q206 and their associated components (Trigger Board).

SYMPTOM 5

Does not sweep, but only with combination of "MIN. DELAY" and "MANUAL" Trigger.

CAUSE

No trigger command from the Manual Trigger Bistable.

CHECK

(1) The Manual Trigger Pushbutton Switch.

(2) The Manual Trigger Bistable Circuit (Odds and Ends Board).

SYMPTOM 6

Does not sweep with combination of "MIN. DELAY" and both "MANUAL" and "EXT." Trigger. Does sweep in "INT." Trigger mode.

CAUSE

Number two input of the Trigger Gate is ineffective.

CHECK

C303 and Q312 (Clock Board).

SYMPTOM 7

Operates properly in "MIN. DELAY", but not with any delay setting other than "MIN.".

CAUSE

Delay Monostable inoperative.

CHECK

Delay Monostable, Q207 through Q213 and associated circuits (Trigger Board).

SYMPTOM 8

Unit sweeps, but output does not respond to applied signal. Zero Control action normal.

CAUSE 1

Signal and sweep not synchronized.

CHECK

Choice of Trigger Mode.

CAUSE 2

Signal Input Channel Amplifiers, A1 or A2, are defective.

CHECK

Q400 through Q405 and their associated components.

SYMPTOM 9

Sweeps, but output does not respond to applied signal or to Zero Control.

CAUSE 1

Amplifier A3 of the Signal Input Channel or amplifiers A4 through A6 of the Signal Output Channel are defective.

CHECK

Signal Channel Amplifiers A3 through A6.

CAUSE 2

Crowbar Circuit continuously grounds the input of the Signal Output Channel.

CHECK 1

The Gate Generator (crowbar control), Q214 through Q216 and associated components (Trigger Board). The Gate Generator may easily be checked by monitoring the "GATE OUT" Jack with an oscilloscope.

CHECK 2

The bistable which controls the Gate Generator, Q321 through Q323 and associated components (Clock Board).

SYMPTOM 10

Input Signal, with necessary noise (if any), appears at the output when a sweep is NOT in progress.

CAUSE

Crowbar Circuit never grounds out the input of the Signal Output Channel.

CHECK

The Gate Generator (Trigger Board) and the Bistable.

SECTION VII
WARRANTY

Princeton Applied Research Corporation warrants each instrument of its own manufacture to be free from defects in material and workmanship. Obligations under this Warranty are limited to replacing, repairing or giving credit for the purchase price, at our option, of any instrument returned prepaid to our factory for that purpose within ONE YEAR of delivery to the original purchaser. Instruments returned to the factory are accepted only when prior authorization has been given by an authorized representative of Princeton Applied Research Corporation.

This Warranty shall not apply to any instrument, which our inspection shall disclose to our satisfaction, to have become defective or unworkable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation, or other causes beyond our control.

Princeton Applied Research Corporation reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is in lieu of, and excludes all other warranties or representations, expressed, implied or statutory, and all other obligations or liabilities of Princeton Applied Research Corporation including special or consequential damages, and no other source is authorized to assume for Princeton Applied Research Corporation any other liability.

SECTION VIII
SCHEMATICS

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VIII-1 ---------- TABLE OF SCHEMATICS

VIII-2 ---------- BLOCK DIAGRAM

VIII-3 ---------- SIGNAL AMPLIFIER BOARD

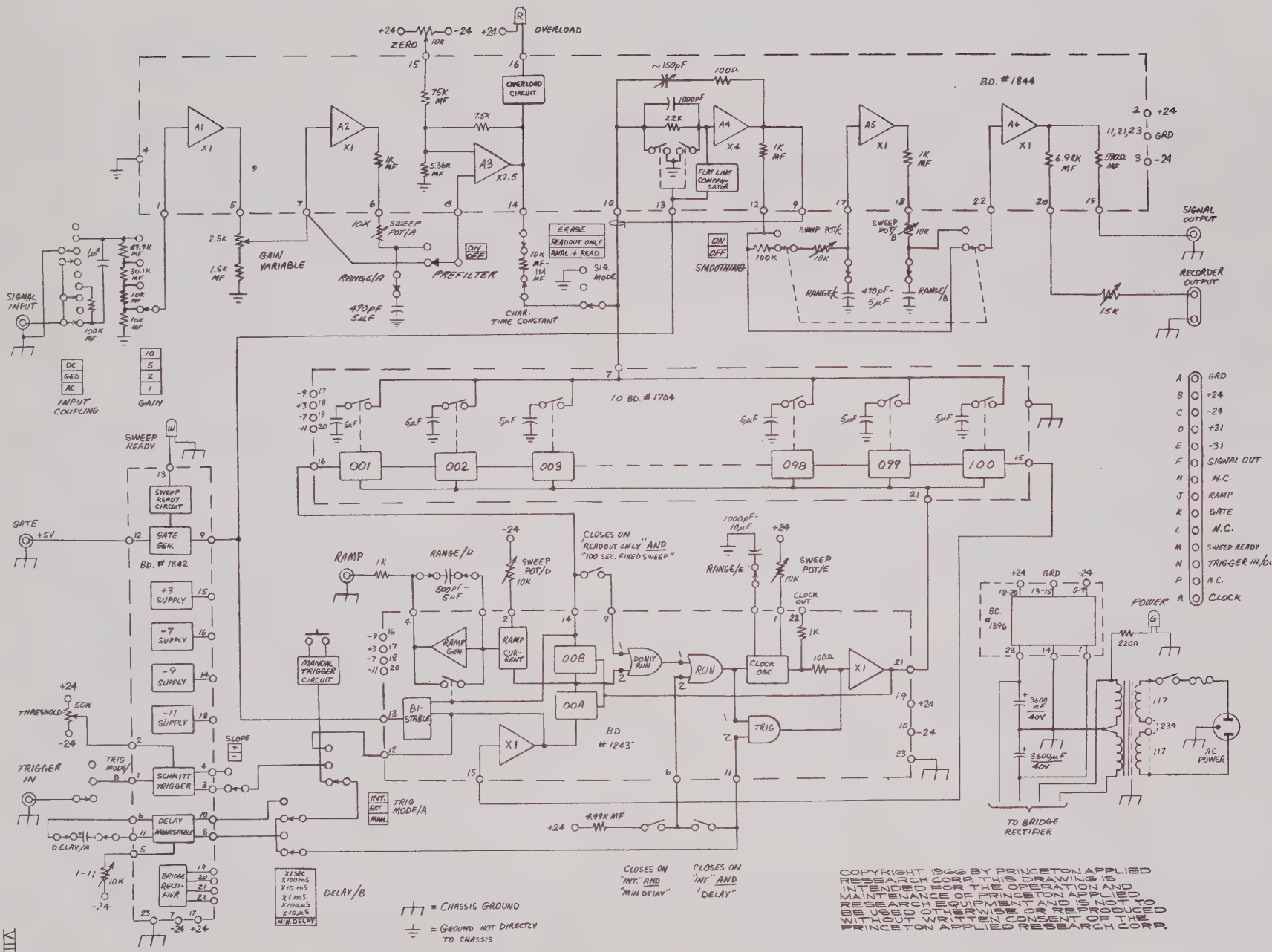
VIII-4 ---------- GATING AND STORAGE BOARD

VIII-5 ---------- CLOCK BOARD

VIII-6 ---------- TRIGGER BOARD

VIII-7 ---------- ±24 V REGULATORS

VIII-8 ---------- CHASSIS WIRING SCHEMATIC



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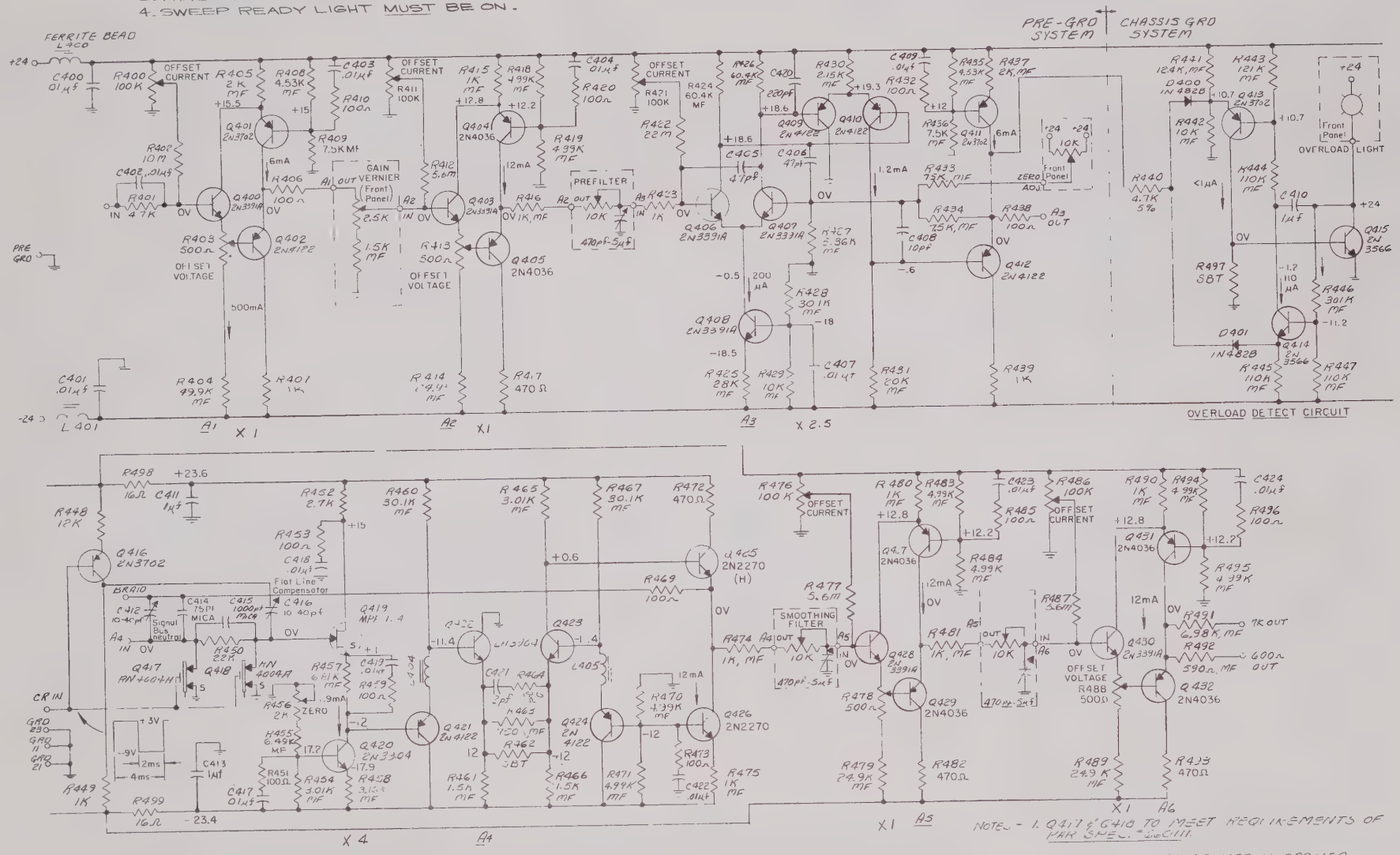
TDH-9 BLOCK DIAGRAM

VOLTAGES INDICATED MEASURED UNDER THE FOLLOWING CONDITIONS:

1. ZERO ADJUSTED FOR ZERO OUT.
2. EXTERNAL TRIGGER MODE BUT NO TRIGGER APPLIED
3. THRESHOLD CONTROL FULLY CLOCKWISE.
4. SWEEP READY LIGHT MUST BE ON.

INDICATED WAVEFORMS OBSERVED UNDER THE FOLLOWING CONDITIONS:

1. OSCILLOSCOPE TRIGGERED FROM THE TDH-9 GATE OUTPUT.
2. EXTERNAL TRIGGERING FROM 250 Hz SINE WAVE.
3. DELAY SET TO ONE MILLISECOND.
4. SWEEP SET TO TWO MILLISECONDS.



NOTE - 1. Q417 & Q418 TO MEET REQUIREMENTS OF MIL SPEC. MIL-S-19500/111.

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CONNECTOR PIN CONNECTIONS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A1 IN	+24	-24	PRE GRD	A1 OUT	A2 OUT	A2 IN	A3 IN	BRAID	A4 IN	GRD	A4 OUT	CR IN BIAS	A5 OUT	ZERO ADJ	OVLD	A6 IN	A6 OUT	600 OUT	7K OUT	GRD	A5 IN	GRD

CIRCUIT BOARD Nº 1844 — SIGNAL AMPLIFIER — MODEL - TDH-9

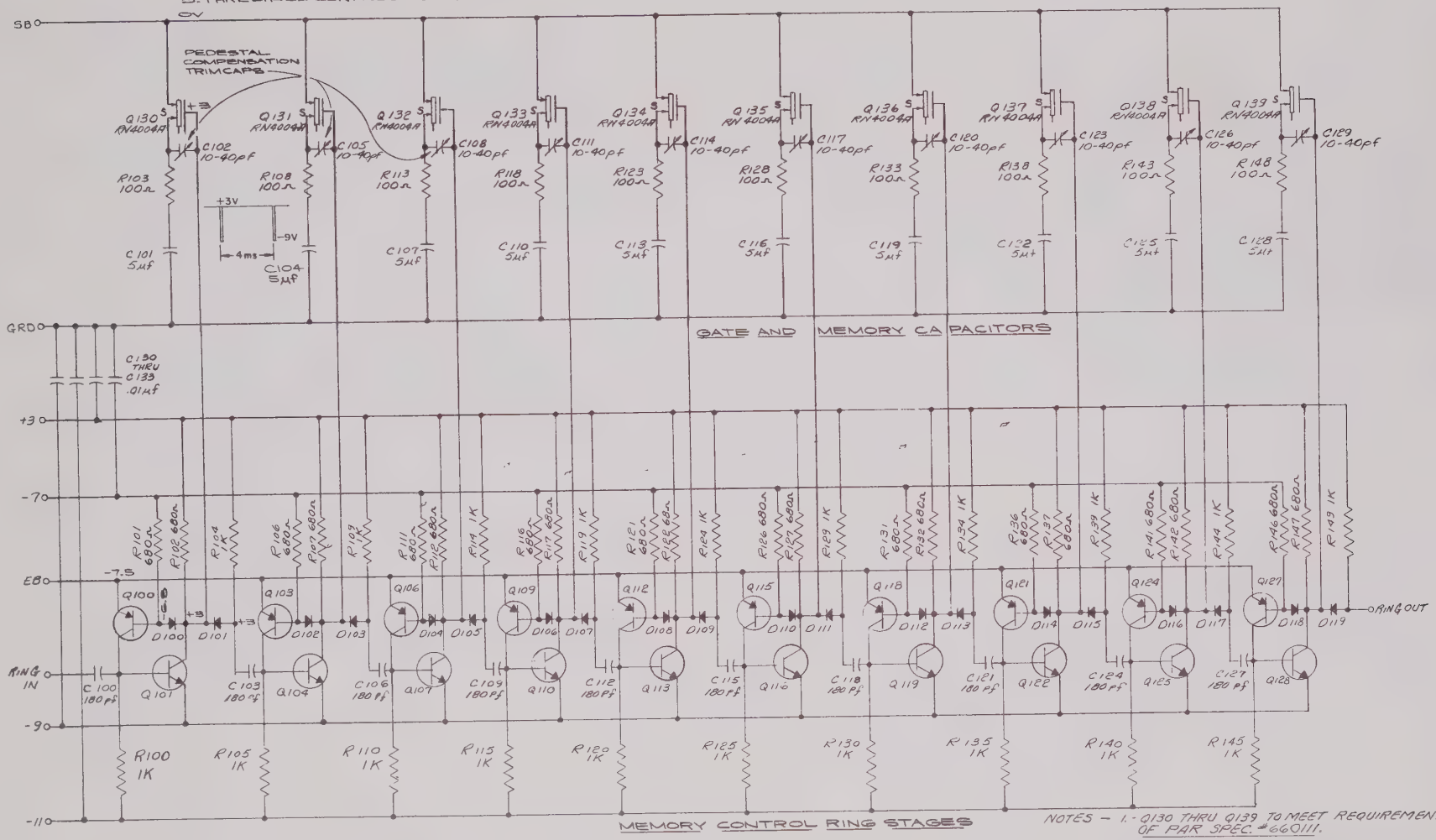
VIII-3

VOLTAGES INDICATED MEASURED UNDER THE FOLLOWING CONDITIONS :

1. ZERO ADJUSTED FOR ZERO OUT.
2. EXTERNAL TRIGGER MODE BUT NO TRIGGER APPLIED.
3. THRESHOLD CONTROL FULLY CLOCKWISE.
4. SWEEP READY LIGHT MUST BE ON.

INDICATED WAVEFORMS OBSERVED UNDER THE FOLLOWING CONDITIONS :

1. OSCILLOSCOPE TRIGGERED FROM THE TDH-9 GATE OUTPUT.
2. EXTERNAL TRIGGERING FROM 250 Hz SINE WAVE.
3. DELAY SET TO ONE MILLISECOND.
4. SWEEP SET TO TWO MILLISECONDS.



NOTES – 1. - Q130 THRU Q139 TO MEET REQUIREMENTS OF PAR SPEC. #660111.

- ALL NPN TRANSISTORS 2N3646, ALL PNP TRANSISTORS 2N3702, AND ALL DIODES IN4009 UNLESS OTHERWISE NOTED.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
NC	NC	NC	NC	NC	NC	SB	NC	NC	NC	NC	NC	NC	NC	RING OUT	RING IN	-9	+3	-7	-11	EB	NC	GRD

CIRCUIT BOARD No. GS 1704 — GATING & STORAGE BOARD — MODEL - TDH-9

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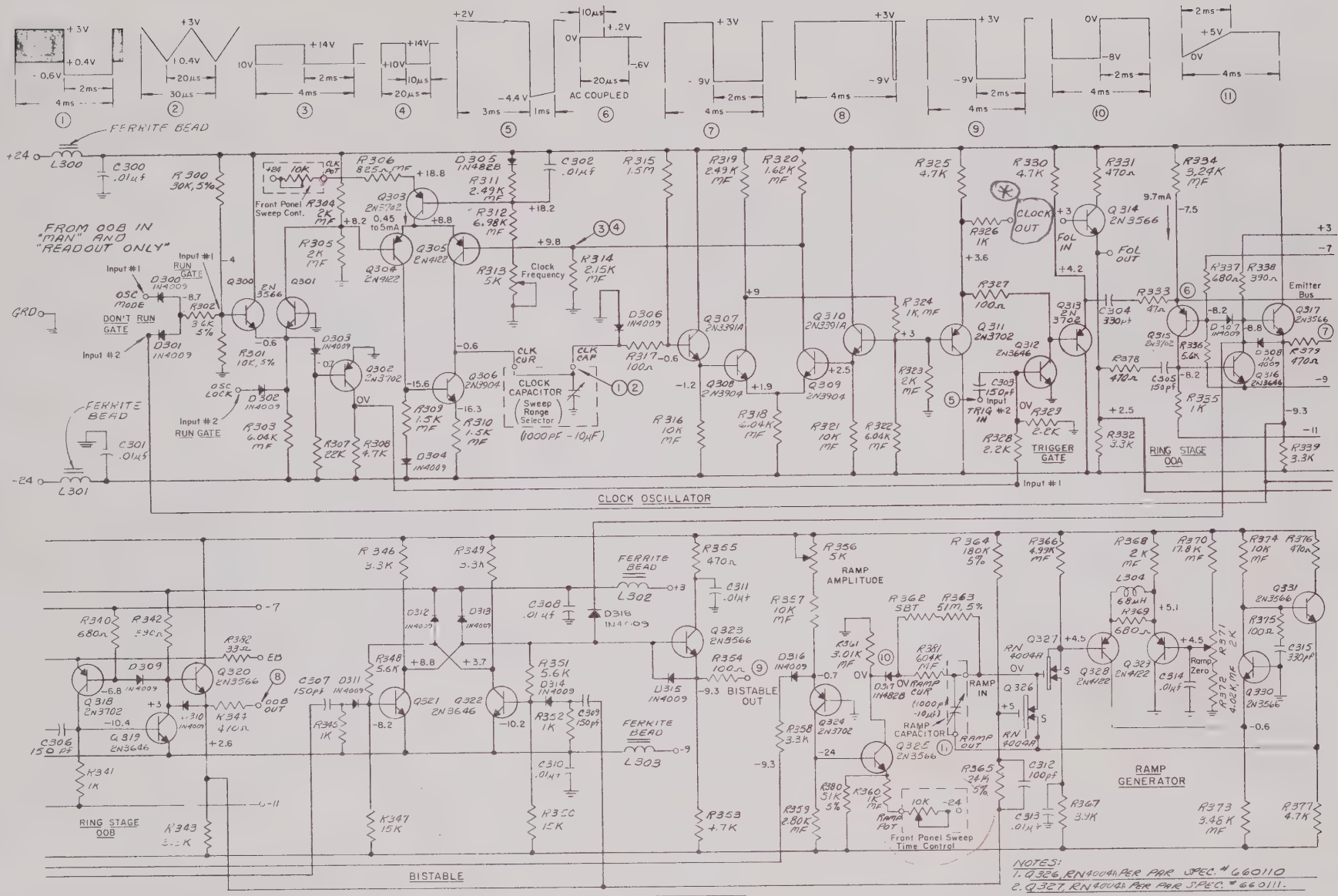
1890 C SD G



1 CLK Pot	2 Ramp Pot	3 Ramp IN	4 Ramp OUT	5 Ramp CUR	6 OSC Lock	7 CLK CUR	8 CLK CAP	9 OSC mode	10 -24	11 TRIG IN	12 FOL OUT	13 BI OUT	14 008 OUT	15 FOL IN	16 -9	17 +3	18 -7	19 +24	20 -11	21 EB	22 CLK OUT	23 GRD

CONNECTOR PIN CONNECTIONS

MODEL TDH-9 CLOCK

NOTES:
1. Q326, RN4004A PER PAR SPEC. # 660110
2. Q327, RN4004A PER PAR SPEC. # 660111.

VOLTAGES INDICATED MEASURED UNDER THE FOLLOWING CONDITIONS:
1. ZERO ADJUSTED FOR ZERO OUT.
2. EXTERNAL TRIGGER MODE BUT NO TRIGGER APPLIED.
3. THRESHOLD CONTROL FULLY CLOCKWISE.
4. SWEEP READY LIGHT MUST BE ON.

INDICATED WAVEFORMS OBSERVED UNDER THE FOLLOWING CONDITIONS:
1. OSCILLOSCOPE TRIGGERED FROM THE TDH-9 GATE OUTPUT.
2. EXTERNAL TRIGGERING FROM 250 Hz SINE WAVE.
3. DELAY SET TO ONE MILLISECOND.
4. SWEEP SET TO TWO MILLISECONDS.

CIRCUIT BOARD No. CL1843

1893 | C | 50 IN

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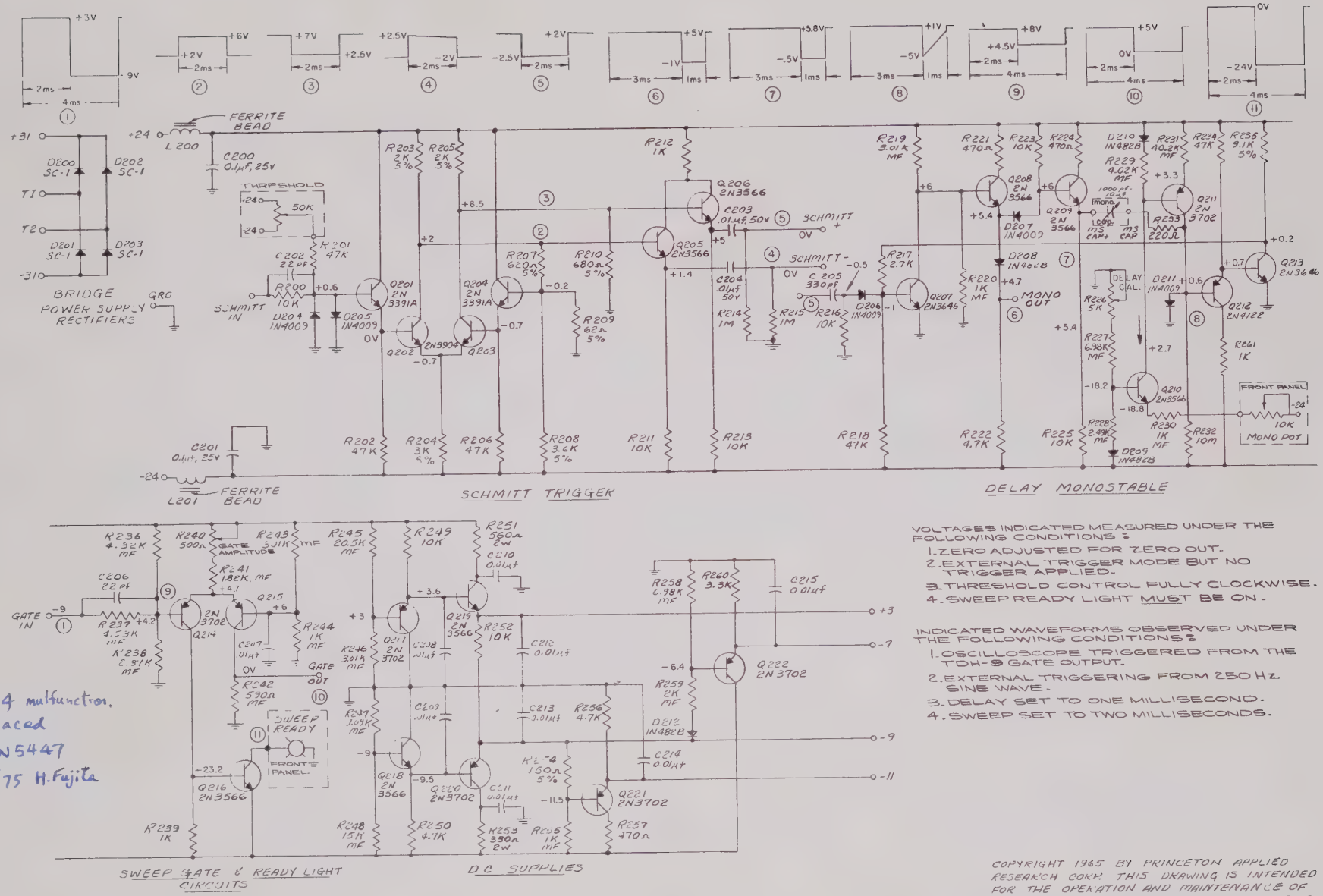

VOLTAGES INDICATED MEASURED UNDER THE FOLLOWING CONDITIONS:

1. ZERO ADJUSTED FOR ZERO OUT.
2. EXTERNAL TRIGGER MODE BUT NO TRIGGER APPLIED.
3. THRESHOLD CONTROL FULLY CLOCKWISE.
4. SWEEP READY LIGHT MUST BE ON.

INDICATED WAVEFORMS OBSERVED UNDER THE FOLLOWING CONDITIONS:

1. OSCILLOSCOPE TRIGGERED FROM THE TDH-9 GATE OUTPUT.
2. EXTERNAL TRIGGERING FROM 250 Hz SINE WAVE.
3. DELAY SET TO ONE MILLISECOND.
4. SWEEP SET TO TWO MILLISECONDS.

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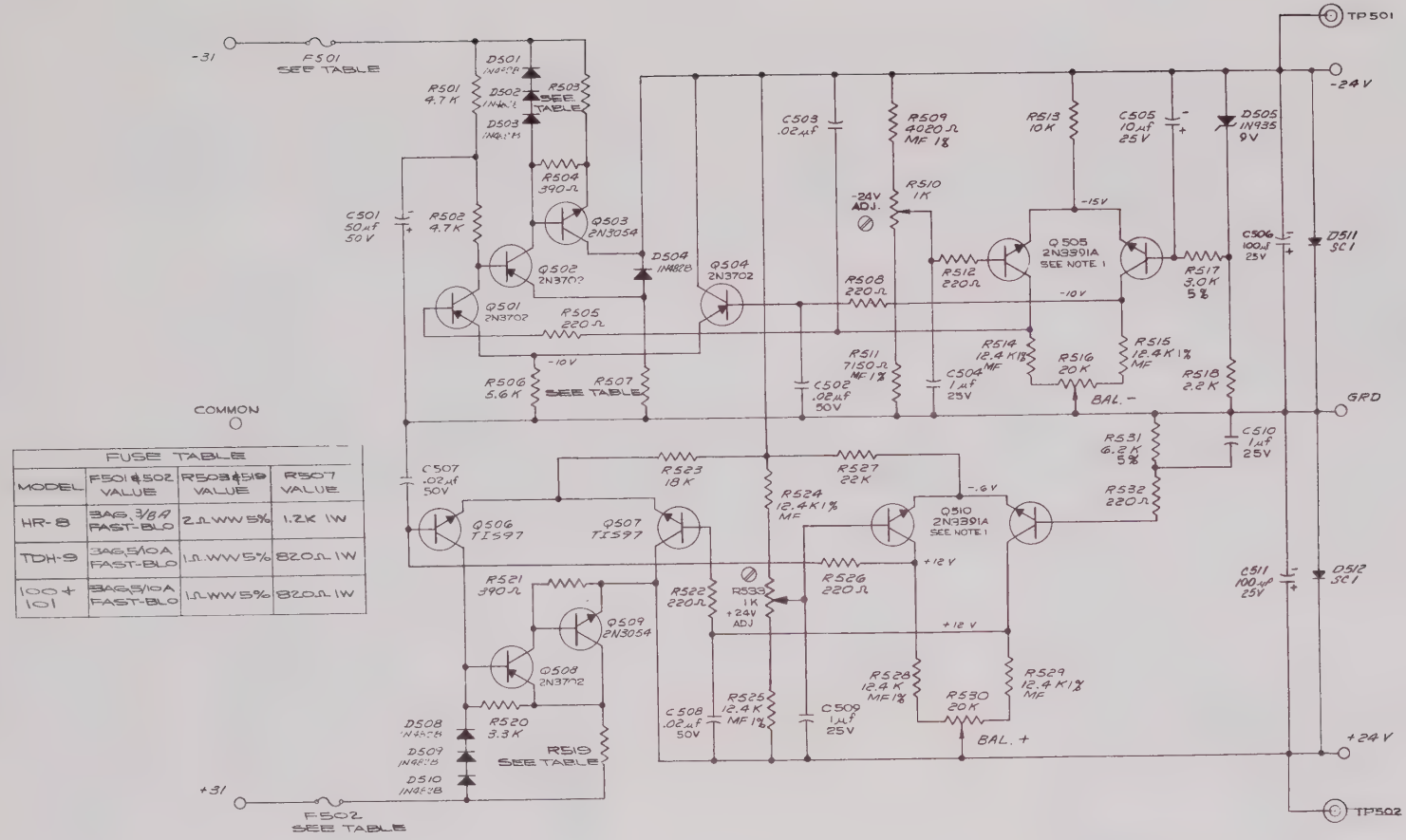
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
SCH IN	SCH BIAS	SCH −	SCH +	MS OUT	MS TAP	-24	MS OUT	GATE IN	MS IN	MS TAP	GATE OUT	SWP RDY	-9	+3	-7	+6.4	-11	T1	-31	T2	+31	GRD

CONNECTOR PIN CONNECTORS

CIRCUIT BOARD No. TR1842 TRIGGER MODEL - TDH-9

1892 | C | SD | F



FUSE TABLE			
MODEL	F501 & 502 VALUE	R503 & 519 VALUE	R507 VALUE
HR-8	3AG, 3/8A FAST-BLO	2.2Ω WW 5%	1.2K 1W
TDH-9	3AG, 5/10A FAST-BLO	1.2Ω WW 5%	820Ω 1W
100 + 101	3AG, 5/10A FAST-BLO	1.2Ω WW 5%	820Ω 1W

NOTE

1. Q 505 & Q510 ARE DIFFERENTIAL PAIR E_{BE} MATCHED @ 100μa (SPEC.# 650412 - GREEN)
2. 2N3711 & TIS97 TRANS. MAY BE SUBSTITUTED FOR 2N3391A TRANS.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
-31	N.C.	N.C.	N.C.	-24	-24	-24	N.C.	N.C.	N.C.	COMMON IN	N.C.	GRD	GRD	GRD	N.C.	N.C.	+24	+24	+24	N.C.	N.C.	+31

CONNECTOR PIN CONNECTIONS

CIRCUIT BOARD Nº. P01396 (HR-8 & TDH-9)
Nº. P01800 (SM-1)

POWER SUPPLIES I & II

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1387 | C | SD | J

CHASSIS WIRING SCHEMATIC TDH-9

POWER SUPPLY
TRIGGER
CLOCK
GATING & STORAGE
SIGNAL
REAR CONNECTOR J7
POWER
PILOT .6V 40MA
S3A
C12 3600 MF 40V
C13 .1 MF
D1 SC-1
D2 SC-1
YEL #91
RED #90
BLK #89
WHT/GRN #74
RED #61
GRN #88
WHT/RED #87
BLU #86
R34 1M
I2 SWEEP READY 28V 40MA
WHT/RED #75
WHT/ORN #72
WHT/RED #64
WHT/RED #79
GRN #78
XI-11
R31
SWP DUR D
R19 10K
R33
THRESHOLD
WHT/RED #84
WHT/RED #83
WHT/YEL #52
WHT/RED #51
ORN #101
YEL #41
V10 #42
GRN #44
ORN #45
RED/ORN #46
RED/GRN #47
C47 100 PF
BLU #48
WHT/BRN #49
R30 1K
RED #61
WHT/BLU #24
WHT/BLK #102
BLU #1
SMOOTHING OFF ON S12
R511 100K
RED #26
WHT/RED #3
GRY #2
RECORDER ADJUST
RECORDER OUTPUT
J6
R5 15K CW
I3 OVERLOAD
28V 40MA
WHT #7
WHT/VIO #6
FINK #5
R4 10K
WHT/BLU #8
ZERO
WHT/GRN #9
WHT/ORN #10
RED #12
J5
WHT/RED #4
SIGNAL OUT
BLK #37
R58 1M MF
R57 402K MF
R7 200K MF
R8 100K MF
R9 40.2K MF
R10 19.1K MF
R11 8.33K MF
C15 .005MF
R6 220Ω
ERASE
SIGNAL MODE S5A
CHAR. TC
500 SEC
200 SEC
100 SEC
50 SEC
20 SEC
10 SEC
5 SEC
S11
PREFILTER OFF ON S13
WHT #107
YEL #4
VIO #16
GAIN
BLK #17
WHT/RED #20
RED #21
GRN #5
WHT/BLK #106
R14 20.9K
R15 30.1K
R16 10K
R17 10K
C16 7-35PF
C17 7-35PF
C18 7-35PF
C43 .005MF
C19 .1MF
R18 100K
YEL #40
J4 INPUT
BLK #67
10 5 2 1 GAIN 59
DC GND 4C INPUT COUPLING S10
R13 5K
WHT/RED #75
WHT/ORN #72
C35 100 MF
C36 10 MF
C37 1 MF
C38 .1 MF
C39 .01 MF
C40 1000 PF
WHT/BLU #76
BLU #80
.01 MF
V0 #77
R36 4.99K MF
WHT/GRN #74
WHT #85
WHT/BLU #98
ORN #83
RED #82
TRIG SLOPE S4
BLU/YEL #96
RED #95
WHT/ORN #92
R37 1MEG
WHT/YEL #93
J1 GATE +5V
J2 TRIG IN
WHT/BLU #97
1 SEC 100 MS 10 MS 1 MS 100 MS 10 MS MANUAL DELAY S3
WHT/YEL #43
INT EXT MAIN TRIG MODE S6
RED #68
SIGNAL MODE 55 B
S7 MAN TRIG
GRN #103
MANUAL TRIGGER PUSHBUTTON SWITCH
R19 10K
RED #62
R27 1.05K MF
R28 174 MF
BLU #63
WHT/ORN #53
1 SEC 100 MS 10 MS 1 MS 100 MS RANGE S8
RED/YEL #50
R26 1K
GRY #60
J3 RAMP
WHT/GRY #55
WHT/RED #65
SWEEP DURATION E
BRN #57
WHT #56
WHT/BLK/ORN #59
WHT/BLK/BRN #58
R25 2K MF
R24 200K MF
47K
SWEEP DURATION A
WHT/GRN #35
WHT/BLU #36
R35 100K
WHT/VIO #18
VIO #19 R19-10K
SWEEP DURATION C
VIO #33
ORN #32
R20 10K
WHT/BLK #28
SWEEP DURATION B
BLU #30
GRN #29
RED #27
YEL #31
WHT/BLK/GRN #34
BRN #11
R19 10K
ORN #22
BLK #66
Q1,Q2-2N3702
MANUAL TRIGGER BISTABLE
ALL SENDS BOARD

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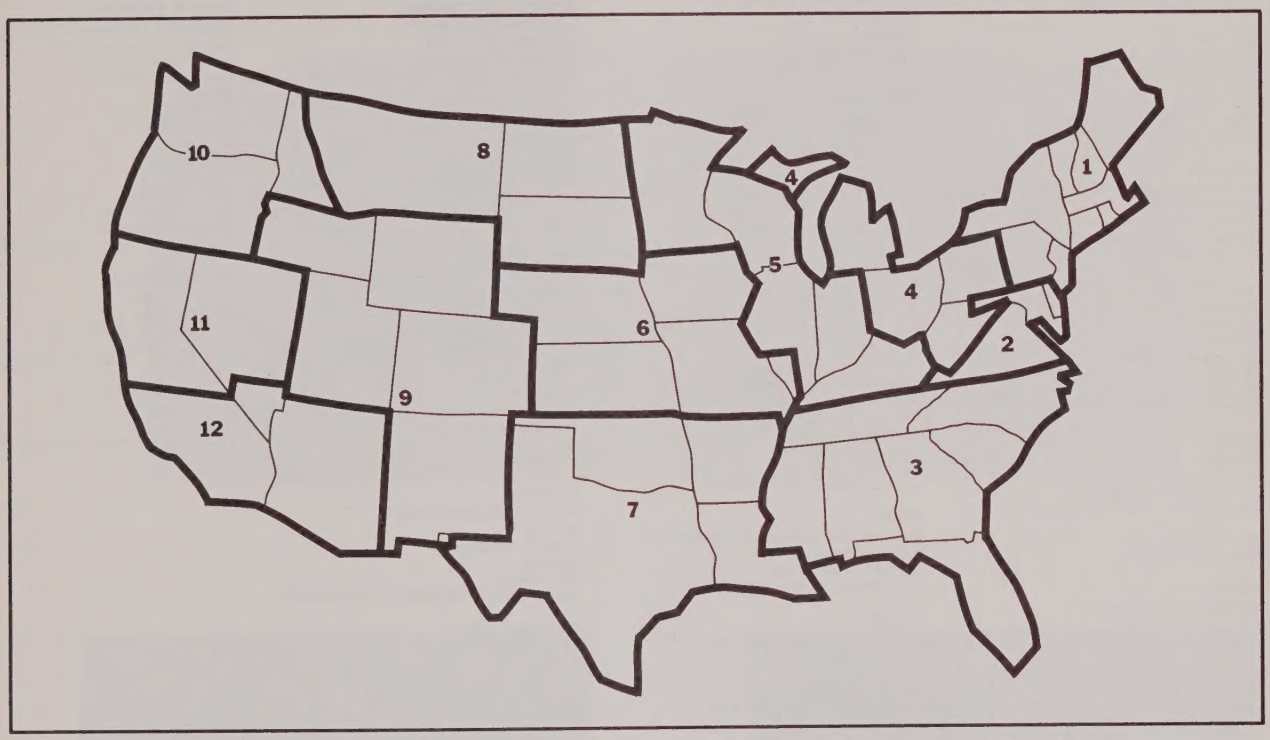

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